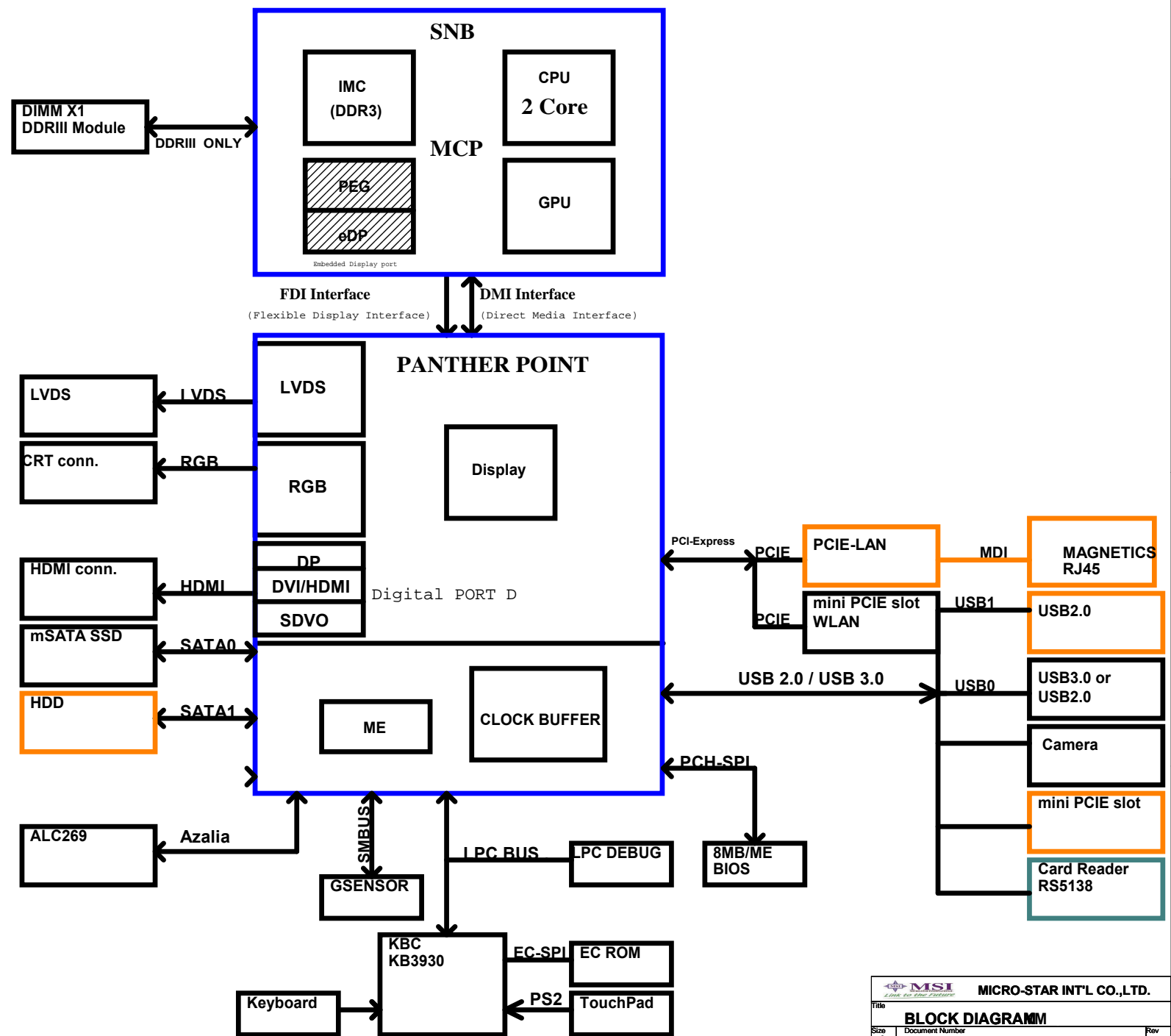



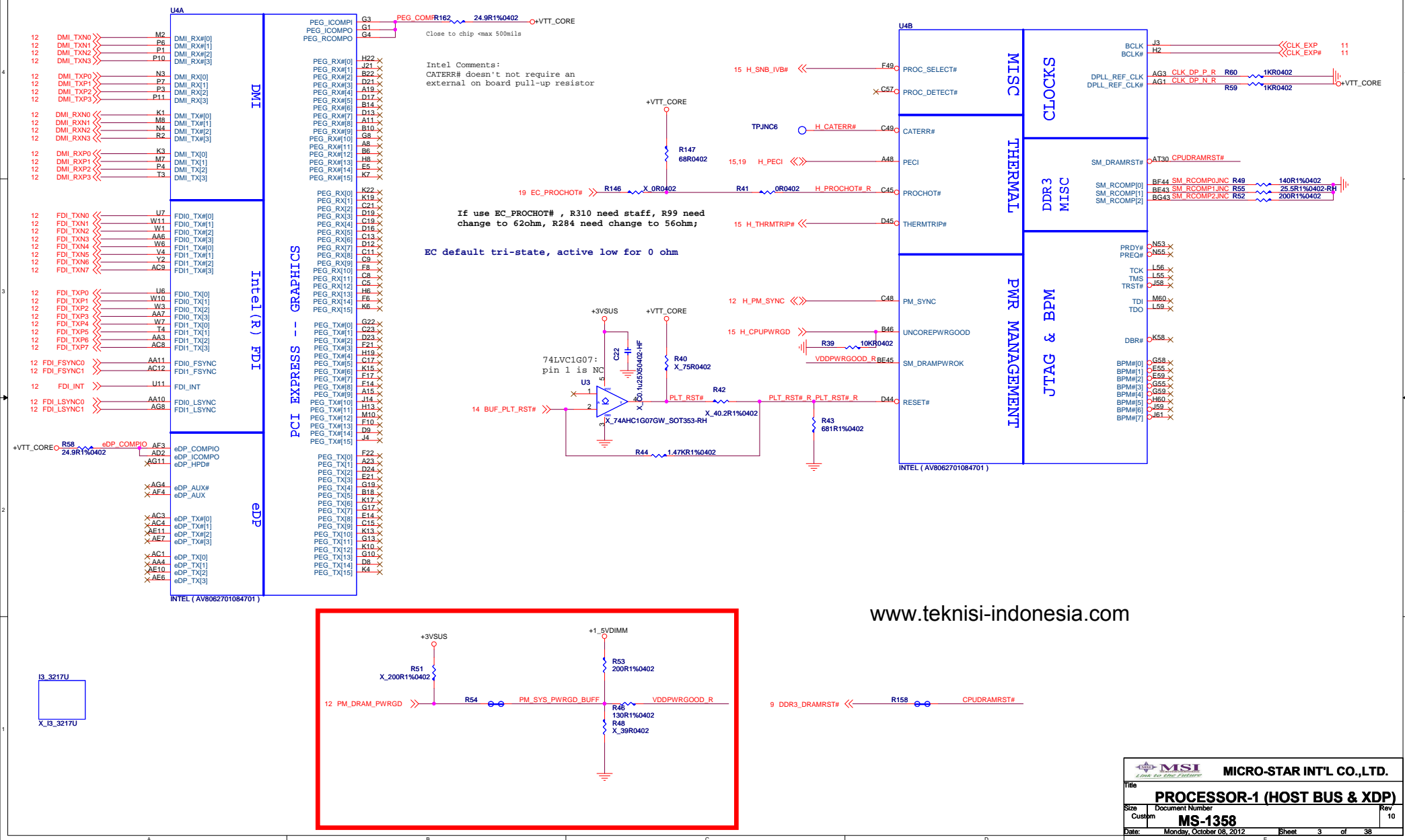
# 1358 VER :10



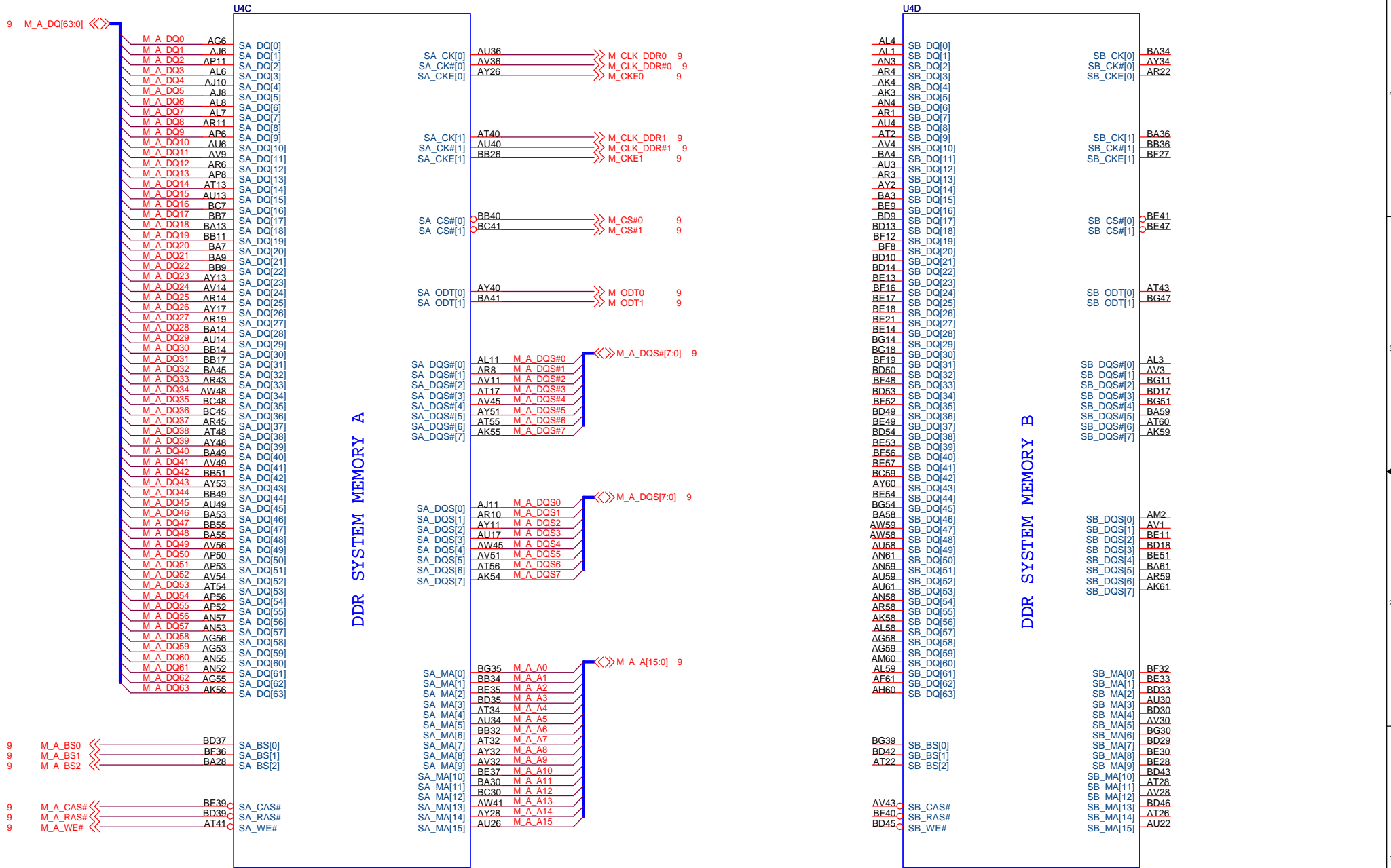
	A	B	C	D	E
1					
2					
3					
4					
	A	B	C	D	E

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>PLATFORM</b>	
Size Custom	Document Number <b>MS-1358</b>
Date: Monday, October 08, 2012	Sheet 2 of 38 Rev 10

IVY BRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)




# IVY BRIDGE 2C BGA PROCESSOR (DDR3)



INTEL ( AV8062701084701 )

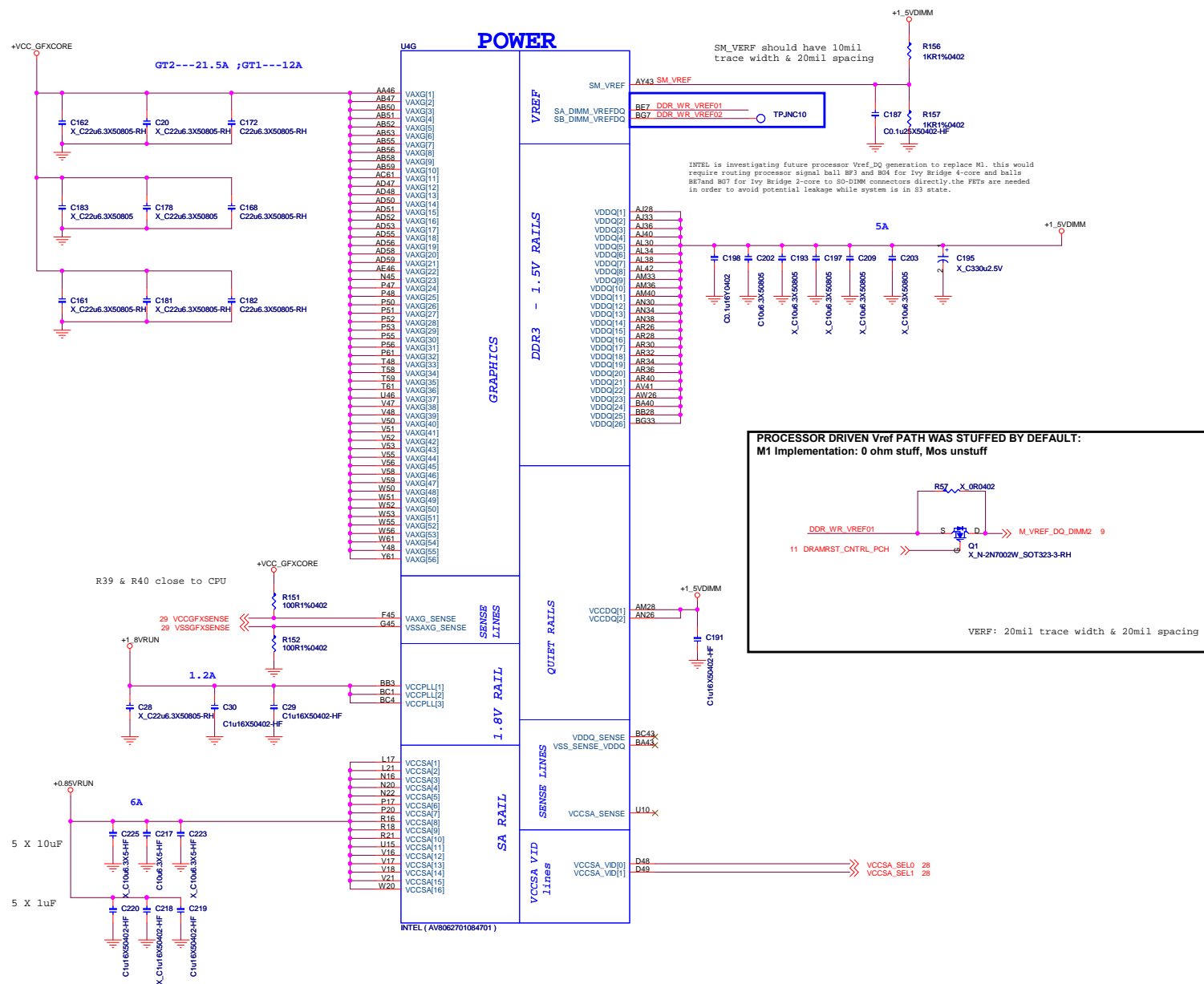
INTEL ( AV8062701084701 )

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>PROCESSOR-2 (DDR3)</b>	
Title Size Custom	Document Number <b>MS-135X</b>
Date: Monday, October 08, 2012	Sheet 4 of 38
Rev 10	

## PEG IO AND DDR IO



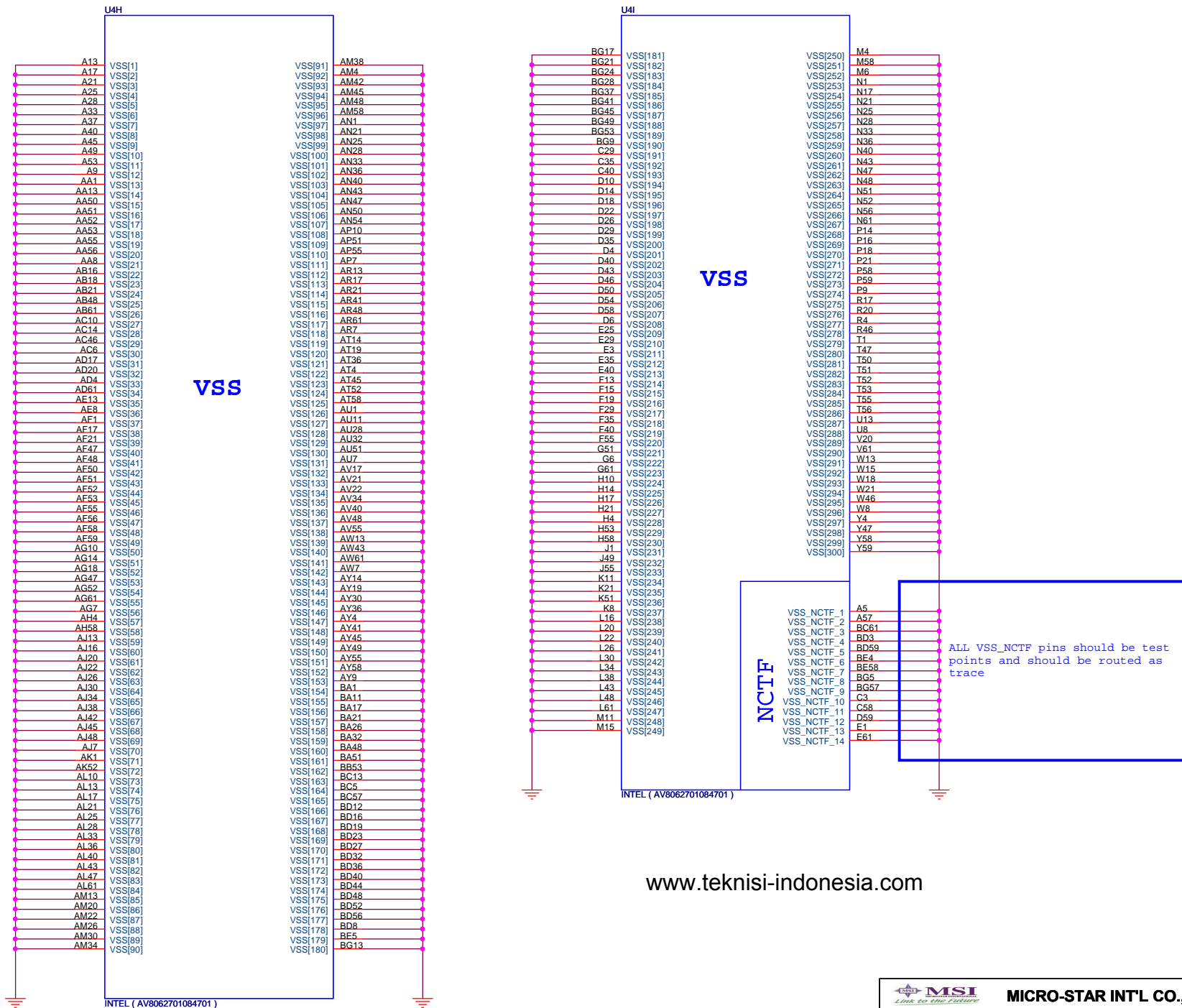
## IVY BRIDGE 2C BGA PROCESSOR (GRAPHICS POWER)




### VCCSA\_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

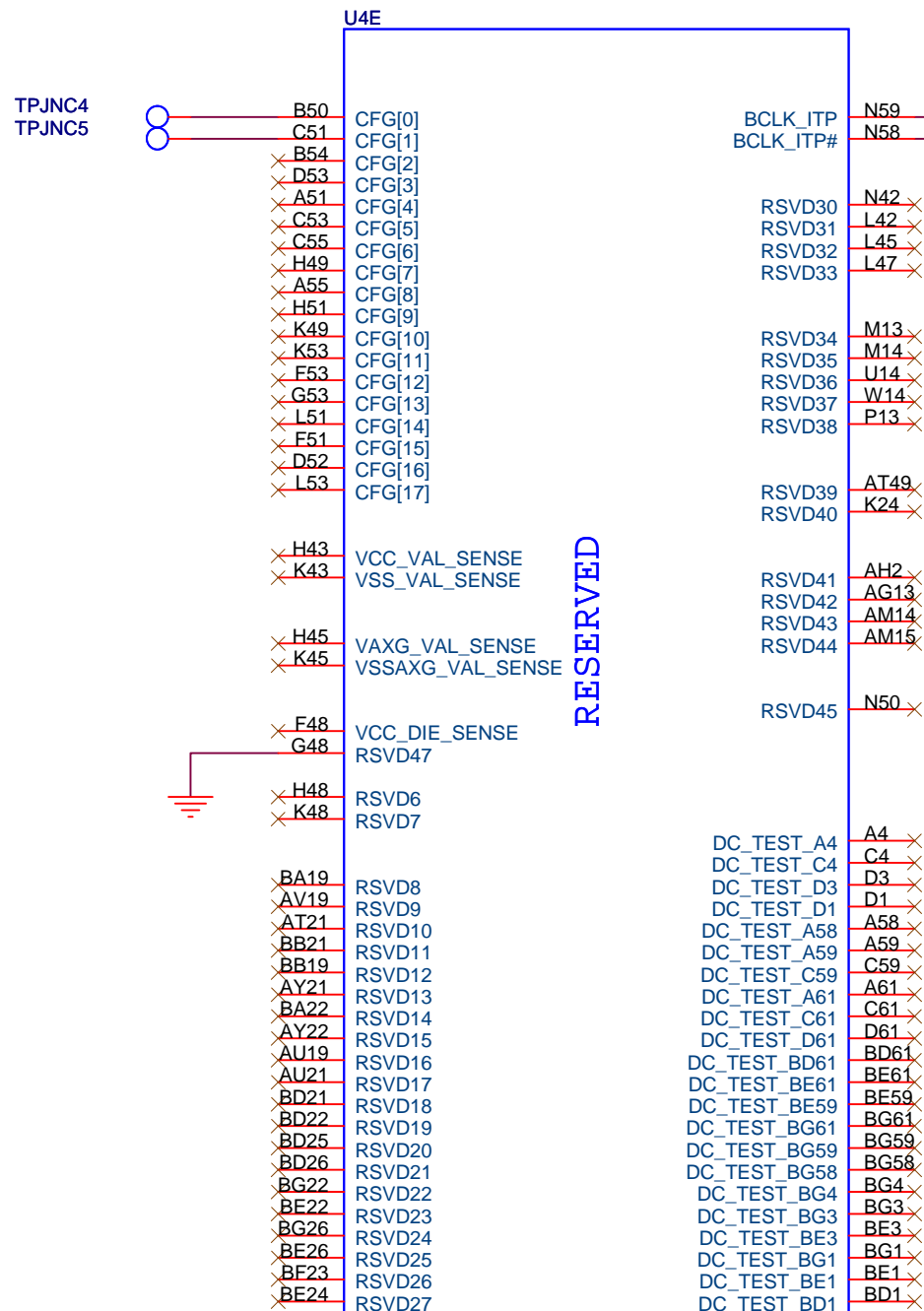
# IVY BRIDGE 2C BGA PROCESSOR (GND)



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 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>PROCESSOR-5 (GND)</b>	
Title Size Custom	Document Number <b>MS-1358</b>
Date: Monday, October 08, 2012	Rev 10


# IVY BRIDGE 2C BGA PROCESSOR (RESERVED)



CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG)  0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K $\pm$ 5% resistor)

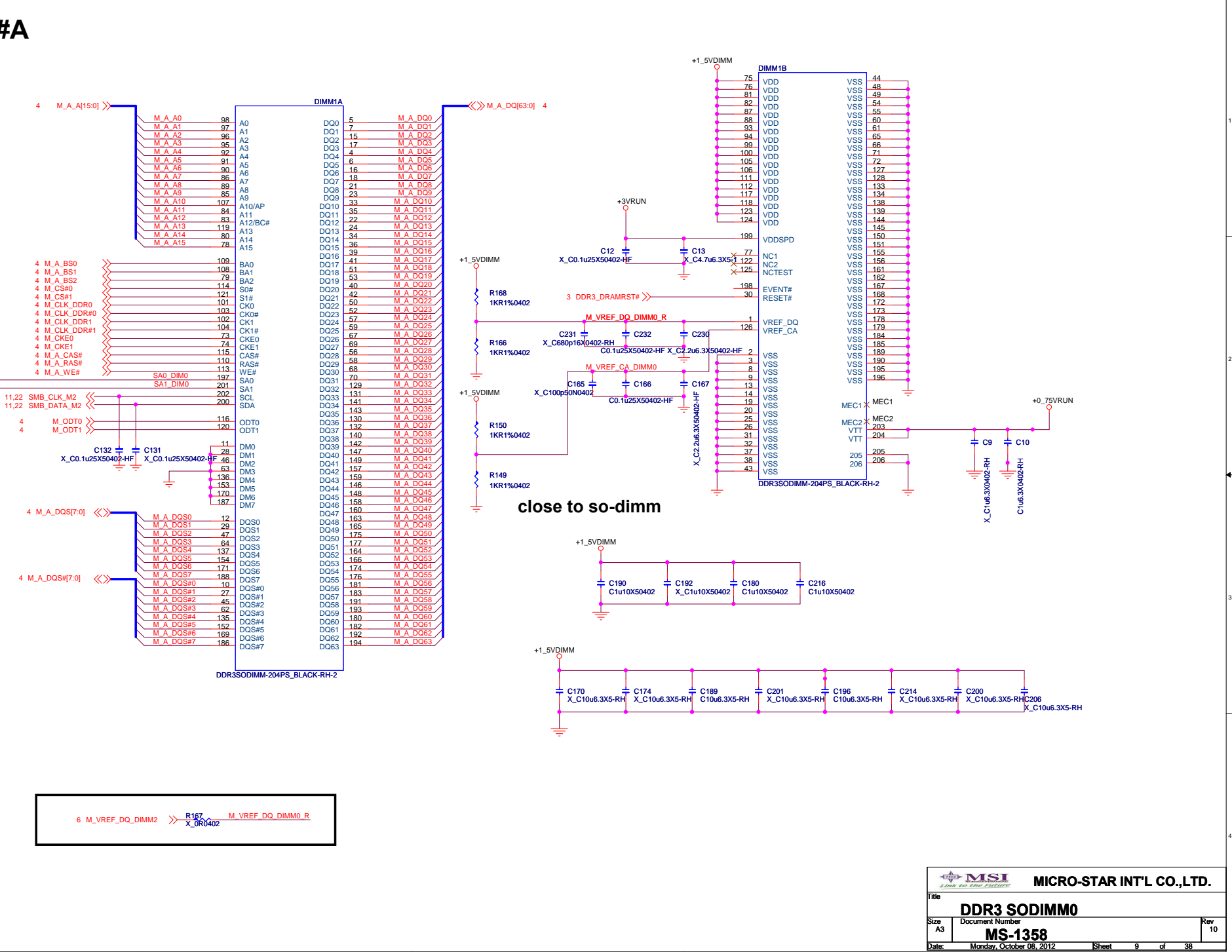
PCI-Express Configuration Select	
CFG[5:6]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express (Default)

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>PROCESSOR-6 (RESERVE)</b>	
Size	Document Number
Custom	<b>MS-1358</b>
Date:	Monday, October 08, 2012
Sheet	8 of 38
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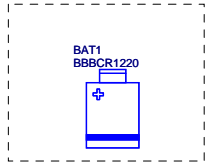
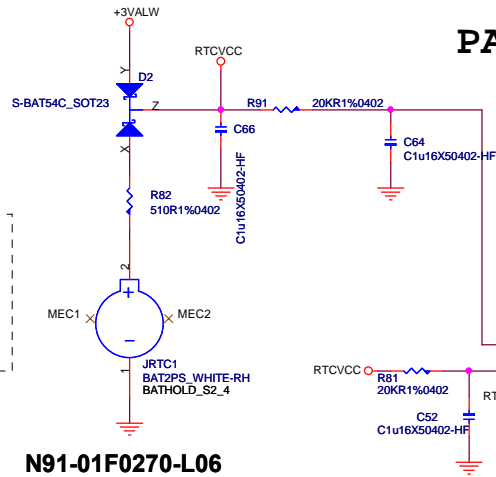
INTEL (AV8062701084701)



A	B	C	D	E
---	---	---	---	---

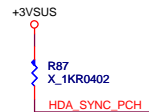


# PANTHER POINT (HDA,JTAG,SATA)



**RTC Battery**  
D06-0101510-K26

**N91-01F0270-L06**



This signal has a weak internal pull-down.  
On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.

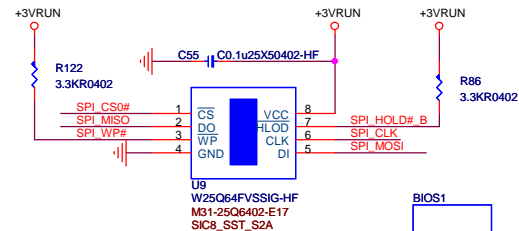
HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V
----------	---

This signal has a weak internal pull-down.  
The strap is sampled on the rising edge of RSMRST# signal.

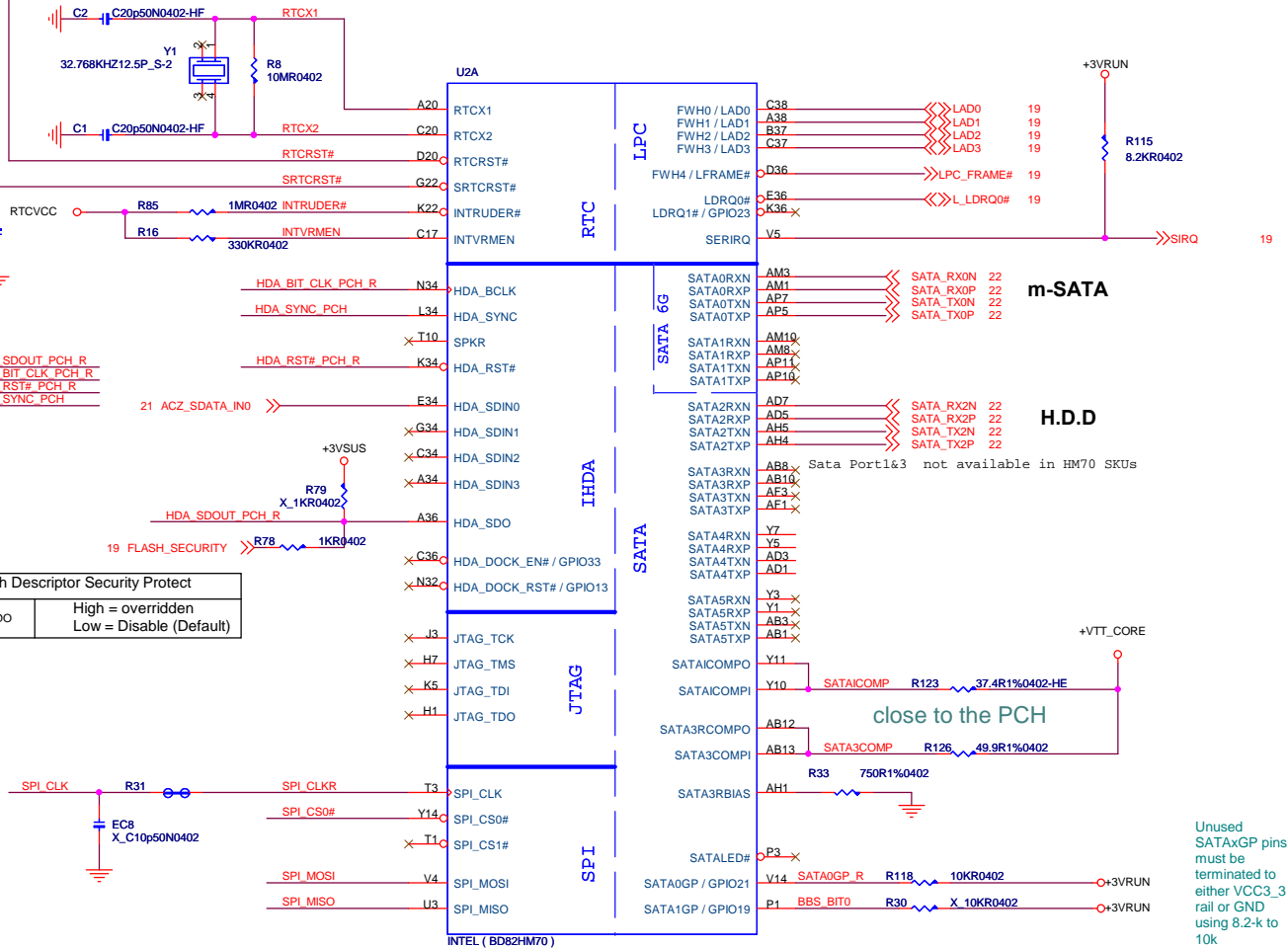
Note: HDA\_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.  
Therefore, platform may need to isolate this signal from the codec during the strap phase.  
Refer to the example circuits provided in the latest Chief River platform design guide.

Flash Descriptor Security Protect	
HDA_SDO	High = overridden Low = Disable (Default)

## EEPROM



**BIOS1**  
X\_W25Q64FVSSIG-HF



**m-SATA**

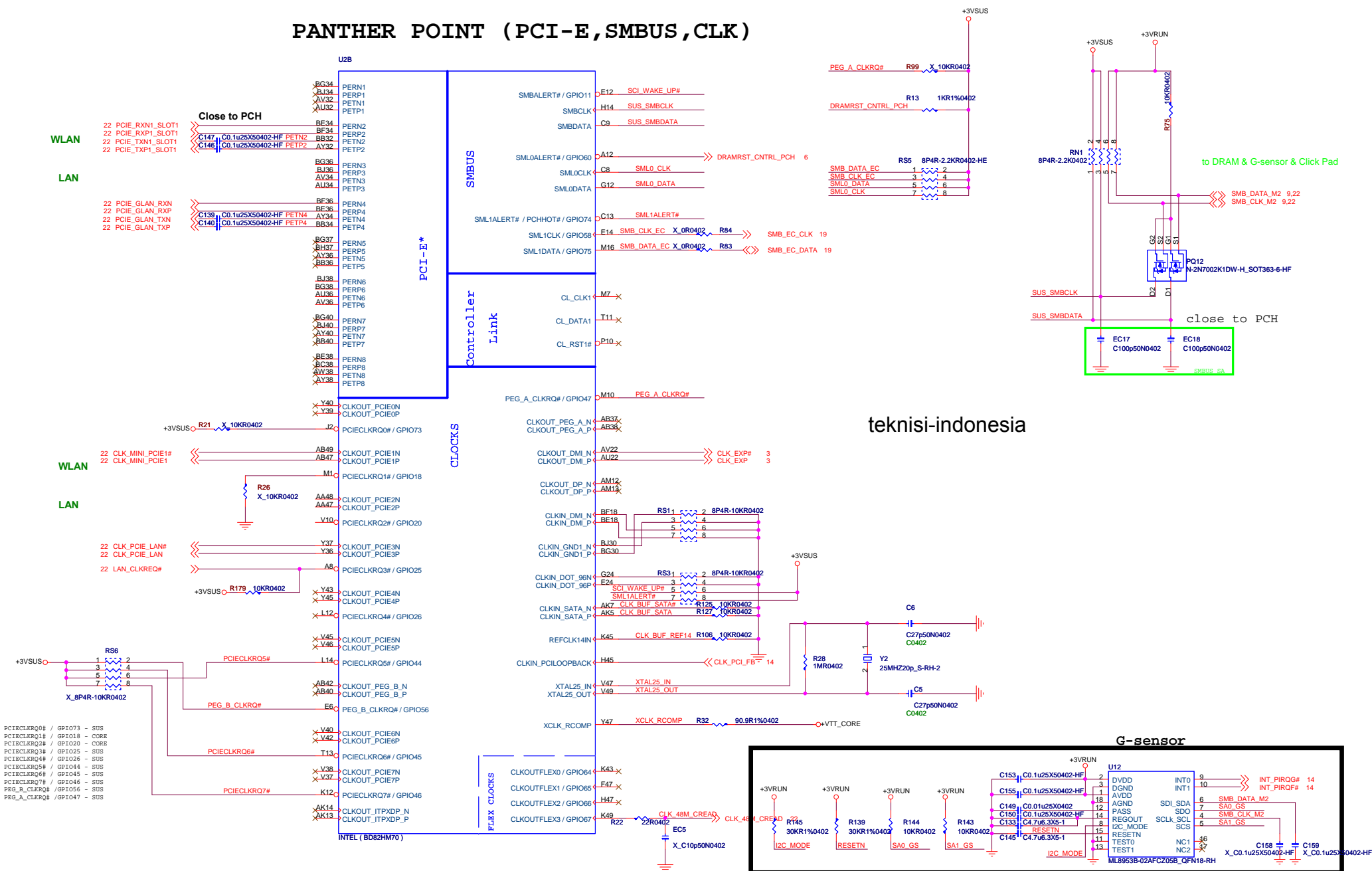
**H.D.D**

close to the PCH

Unused SATAxGP pins must be terminated to either VCC3\_3 rail or GND using 8.2-k to 10k

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)
-----	---

# PANTHER POINT (PCI-E,SMBUS,CLK)

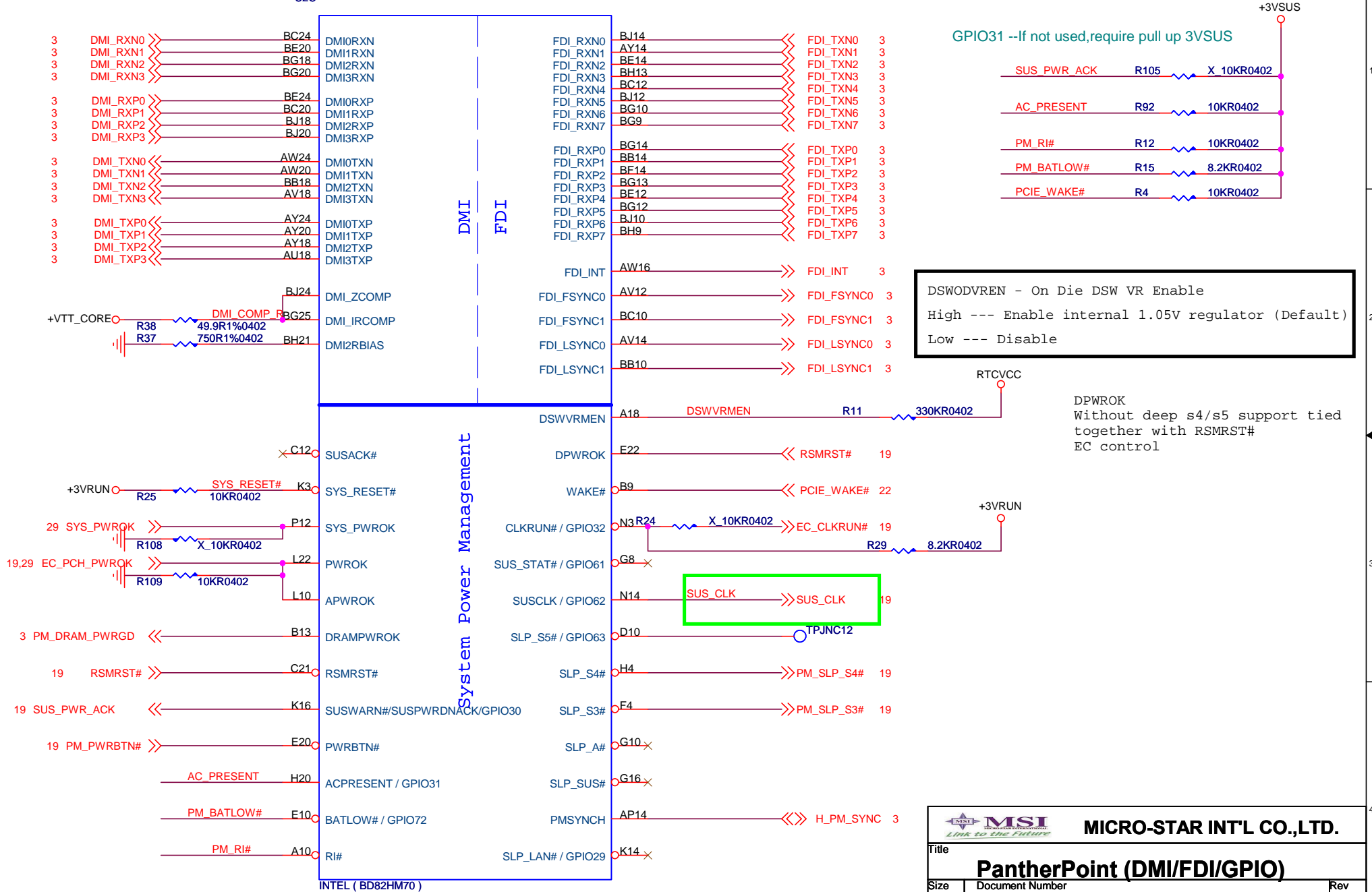



PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.  
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k  $\pm$  10% external pull-up resistor instead of No  
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

Intel Comments:  
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.

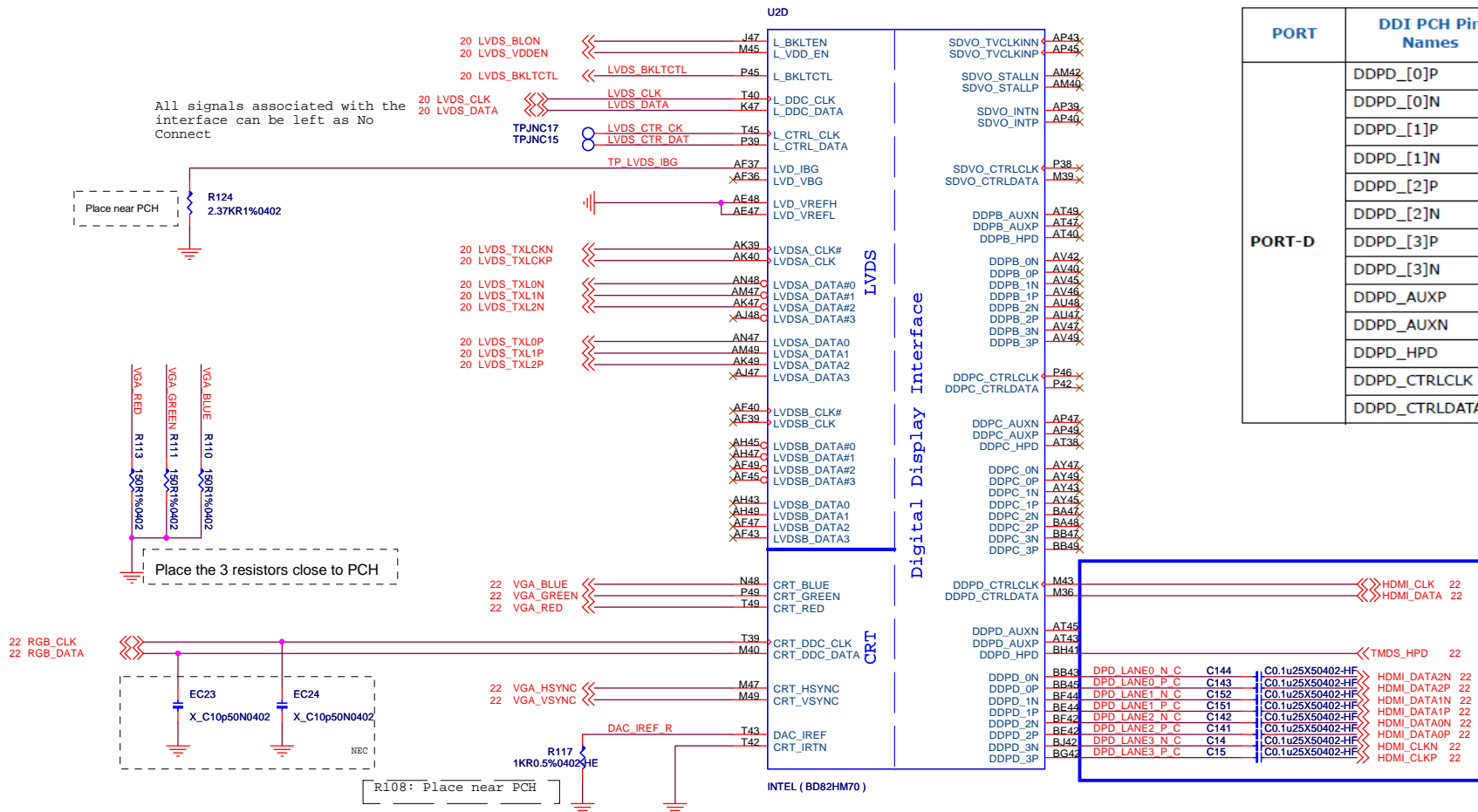
# PANTHER POINT (DMI, FDI, GPIO)

U2C



 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>PantherPoint (DMI/FDI/GPIO)</b>	
<b>Size</b> Custom	<b>Document Number</b> <b>MS-1358</b>
<b>Date:</b> Monday, October 08, 2012	<b>Sheet</b> 12 <b>of</b> 38
<b>Rev</b> 10	

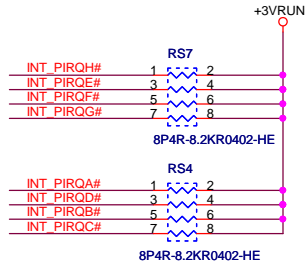
## PANTHER POINT (LVDS,DDI)



PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-D	DDPD_[0]P	TMDSD_DATA2
	DDPD_[0]N	TMDSD_DATA2#
	DDPD_[1]P	TMDSD_DATA1
	DDPD_[1]N	TMDSD_DATA1#
	DDPD_[2]P	TMDSD_DATA0
	DDPD_[2]N	TMDSD_DATA0#
	DDPD_[3]P	TMDSD_CLK
	DDPD_[3]N	TMDSD_CLK#
	DDPD_AUXP	NA
	DDPD_AUXN	NA
	DDPD_HPD	HDMID_HPD
	DDPD_CTRLCLK	HDMID_CTRLCLK
	DDPD_CTRLDATA	HDMID_CTRLDATA

C143					HDMI_CLK	22
C146					HDMI_DATA	22
C45						
C147					TMDS_HPD	22
C148	DPD_LANE0_N_C	C144	C0.1u25X50402-HF			
C149	DPD_LANE0_P_C	C143	C0.1u25X50402-HF		HDMI_DATA2N	22
C150	DPD_LANE1_N_C	C152	C0.1u25X50402-HF		HDMI_DATA1N	22
C151	DPD_LANE1_P_C	C151	C0.1u25X50402-HF		HDMI_DATA1P	22
C152	DPD_LANE2_N_C	C142	C0.1u25X50402-HF		HDMI_DATA0P	22
C153	DPD_LANE2_P_C	C141	C0.1u25X50402-HF		HDMI_DATA0N	22
C154	DPD_LANE3_N_C	C14	C0.1u25X50402-HF		HDMI_CLKP	22
C155	DPD_LANE3_P_C	C15	C0.1u25X50402-HF		HDMI_CLKP	22

# PANTHER POINT (PCI,USB,NVRAM)

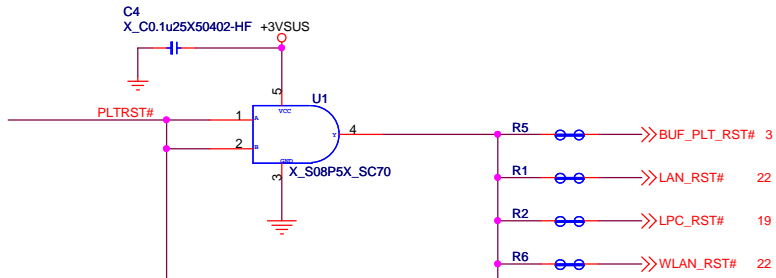
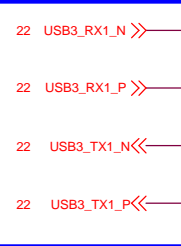


USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

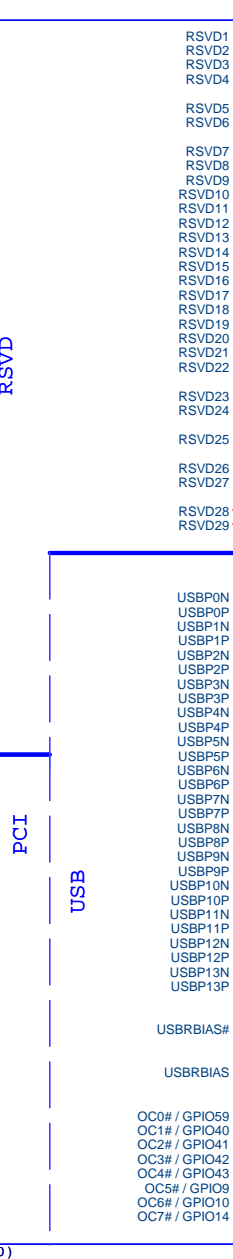
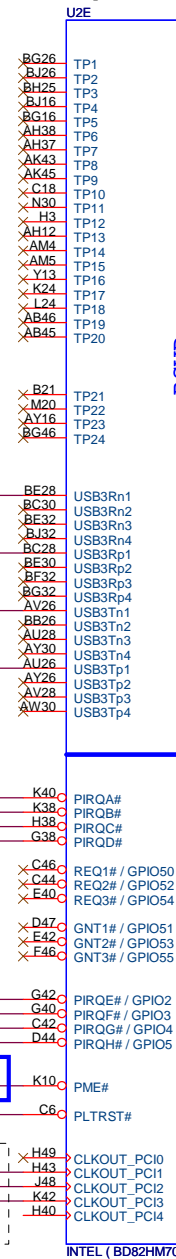
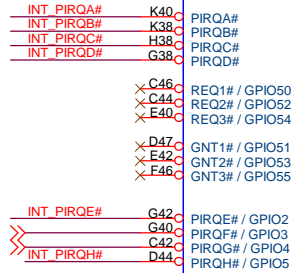
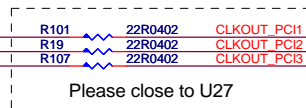
Boot BIOS Strap		
BBS_BIT1 GPIO51	BBS_BIT0 GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Unsupported
1	1	SPI



11 CLK\_PCI\_FB

19 CLK\_PCI\_KBC

19 CLK\_PCI\_PORT80



GPIO35 --Define to EDID Select (If not used,require pull down)

RS8 X 8P4R-10KR0402

R27 X 10KR0402 GPIO39

R23 X 10KR0402 STP\_PCIF#

1 2

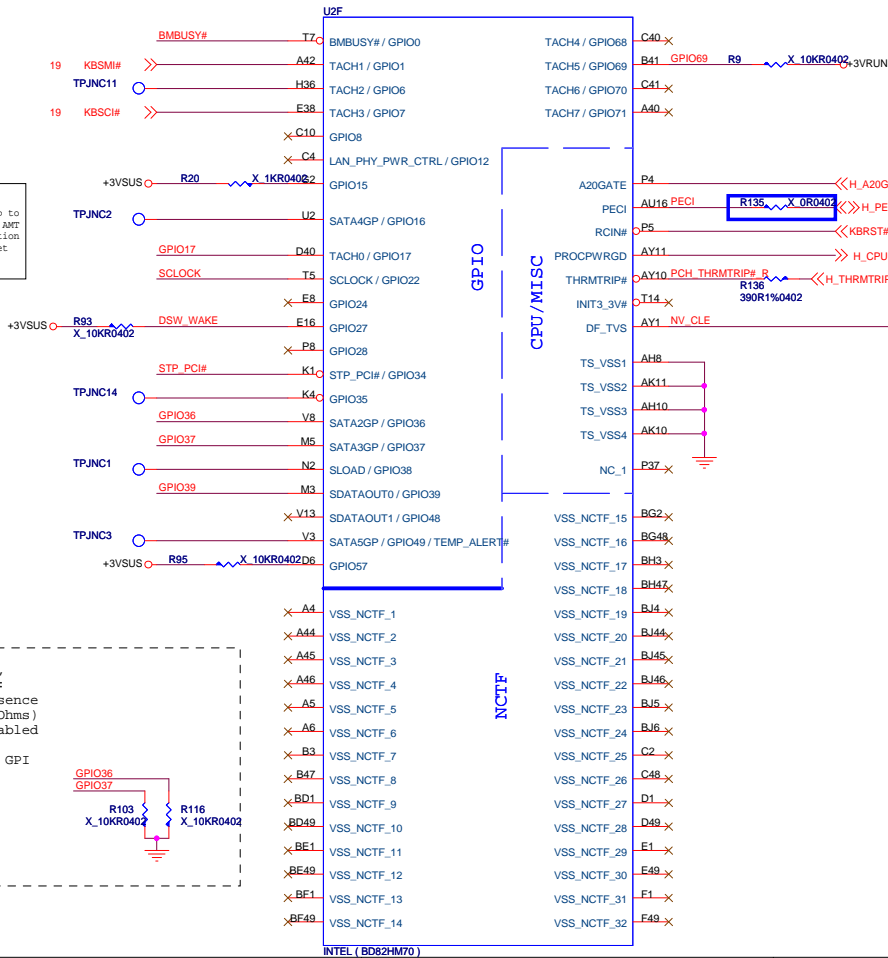
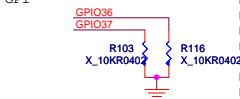
3 4 BMBUSY#

5 6 SCLOCK

7 8 GPIO17

This signal must be pulled up to support Intel RPAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.


```
Since Pin has strap functionality that requires -----
internal pull-down to be sampled at rising PWROK,
following guidelines are required to be followed:
" When Used as SATA2GP/SATA3GP for Mechanical Presence
detect - Use a weak external pull-up (150K-200 Kohms)
to Vcc3_3 OR use 10K external pull-up that is enabled
only after PLTRST# de-assertion.
" When Used as GPIO (Pin# default) - Ensure GPI
is not driven high during strap sampling window
" When Unused as GPIO or SATA*GP - Use 8.2K-10K
pull-down to ground.
```

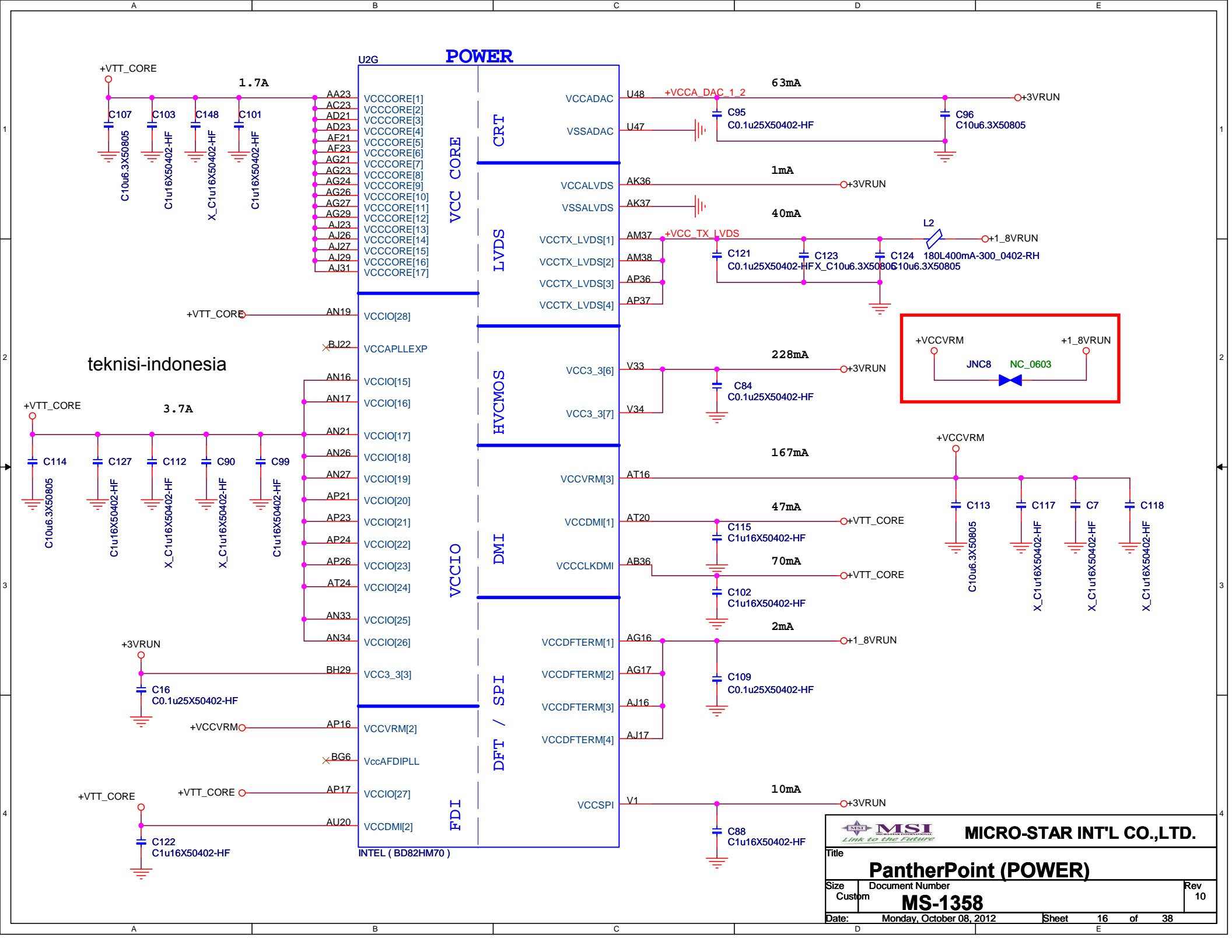


For Ivy Bridge processor only implementation:  
Connect DF\_TVS signal of the PCH to PROC\_SELECT# of the processor  
through a 1K  $\pm$  5% series resistor.  
PROC\_SELECT# also needs a 2.2K  $\pm$  5% pull up resistor to PCH VccDFTERM  
rail.

Intel Comments:  
Reserve 0 ohm option in these pins  
pins AH8, AK11, AH10 & AK10) to GND.

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>PantherPoint (GPIO/NCTF/RSVD)</b>	
<b>Size</b> Custom	<b>Document Number</b> <b>MS-1358</b>
<b>Date:</b> Monday, October 08, 2012	<b>Sheet</b> 15 <b>of</b> 38
<b>Rev</b> 10	



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+VTT\_CORE

+VTT\_CORE

+VCCVRM

+3VRUN

+VTT\_CORE

3.7A

+VTT\_CORE

1.7A

+VTT\_CORE

## POWER

U2G

VCC CORE

CRT

LVDS

HVCMOS

VCCIO

DMI

DFT / SPI

FDI

INTEL ( BD82HM70 )

VCCADAC

VSSADAC

VCCALVDS

VSSALVDS

VCCTX\_LVDS[1]

VCCTX\_LVDS[2]

VCCTX\_LVDS[3]

VCCTX\_LVDS[4]

VCC3\_3[6]

VCC3\_3[7]

VCCVRM[3]

VCCDMI[1]

VCCCLKDMI

VCCDFTERM[1]

VCCDFTERM[2]

VCCDFTERM[3]

VCCDFTERM[4]

VCCSPI

U48

+VCCA\_DAC\_1\_2

63mA

+3VRUN

U47



C95

C0.1u25X50402-HF



C96

C10u6.3X50805

1mA

+3VRUN

AK36

AK37



40mA

L2

+1\_8VRUN

AM37

AM38

AP36

AP37

+VCC\_TX\_LVDS

C121

C0.1u25X50402-HF

X\_C10u6.3X50805

C123

C124

180L400mA-300\_0402-RH

C10u6.3X50805

+VCCVRM

JNC8

NC\_0603

+1\_8VRUN

V33

V34

228mA

+3VRUN

C84

C0.1u25X50402-HF

167mA

+VCCVRM

AT16

AT20

AB36

47mA

+VTT\_CORE

C115

C1u16X50402-HF

70mA

+VTT\_CORE

C102

C1u16X50402-HF

2mA

+1\_8VRUN

AG16

AG17

AJ16

AJ17

C109

C0.1u25X50402-HF


10mA

+3VRUN

V1

C88

C1u16X50402-HF

**MICRO-STAR INT'L CO.,LTD.**

Title

**PantherPoint (POWER)**

SizeCustom

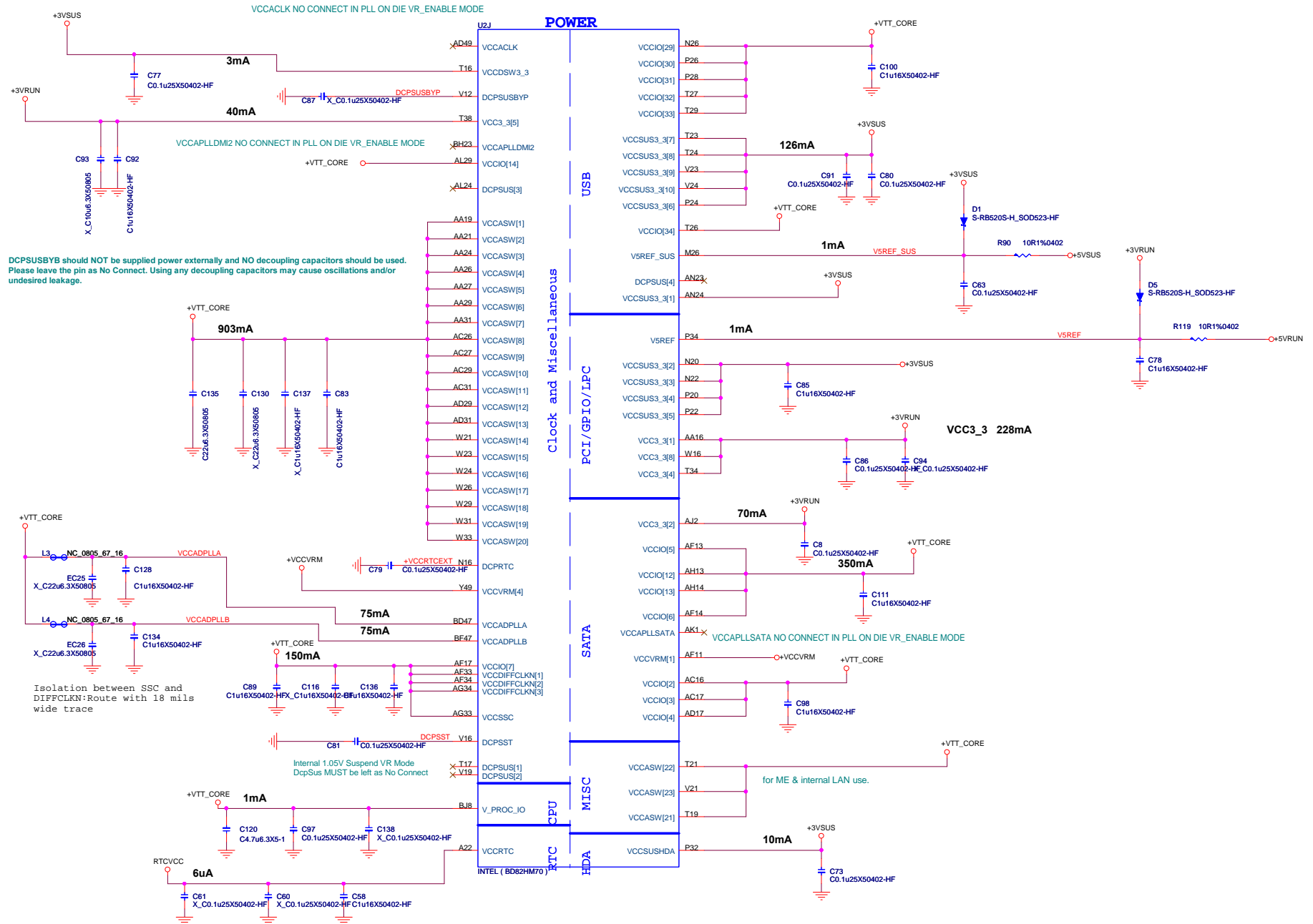
Document Number**MS-1358**

Rev10

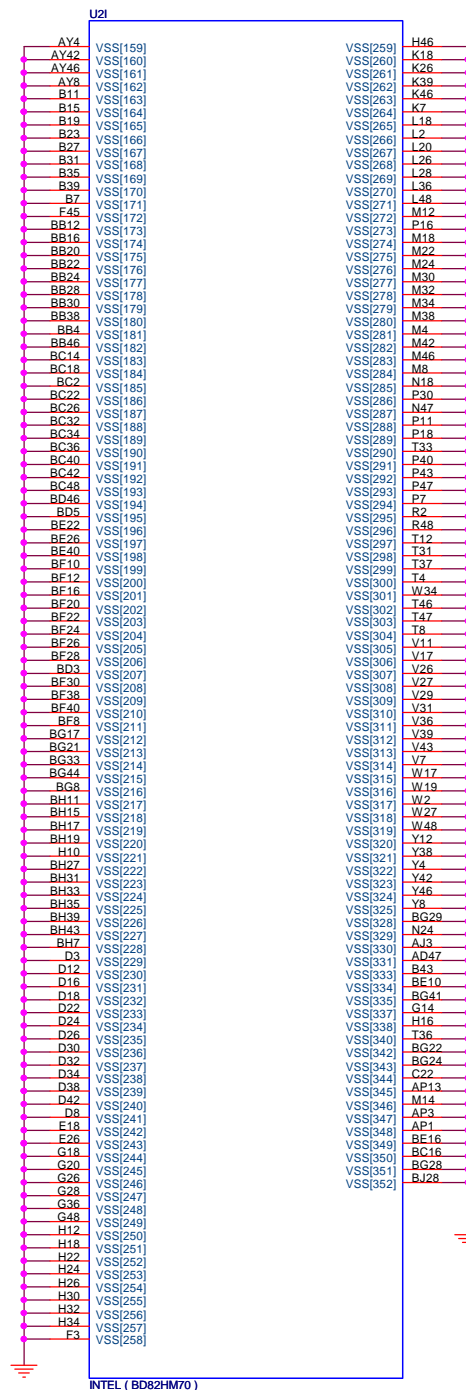
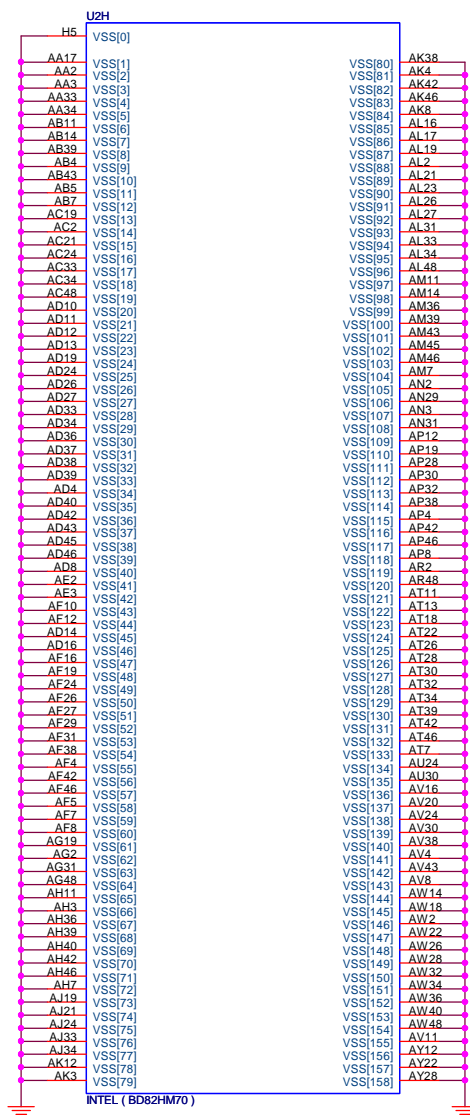
Date:Monday, October 08, 2012Sheet16 of 38

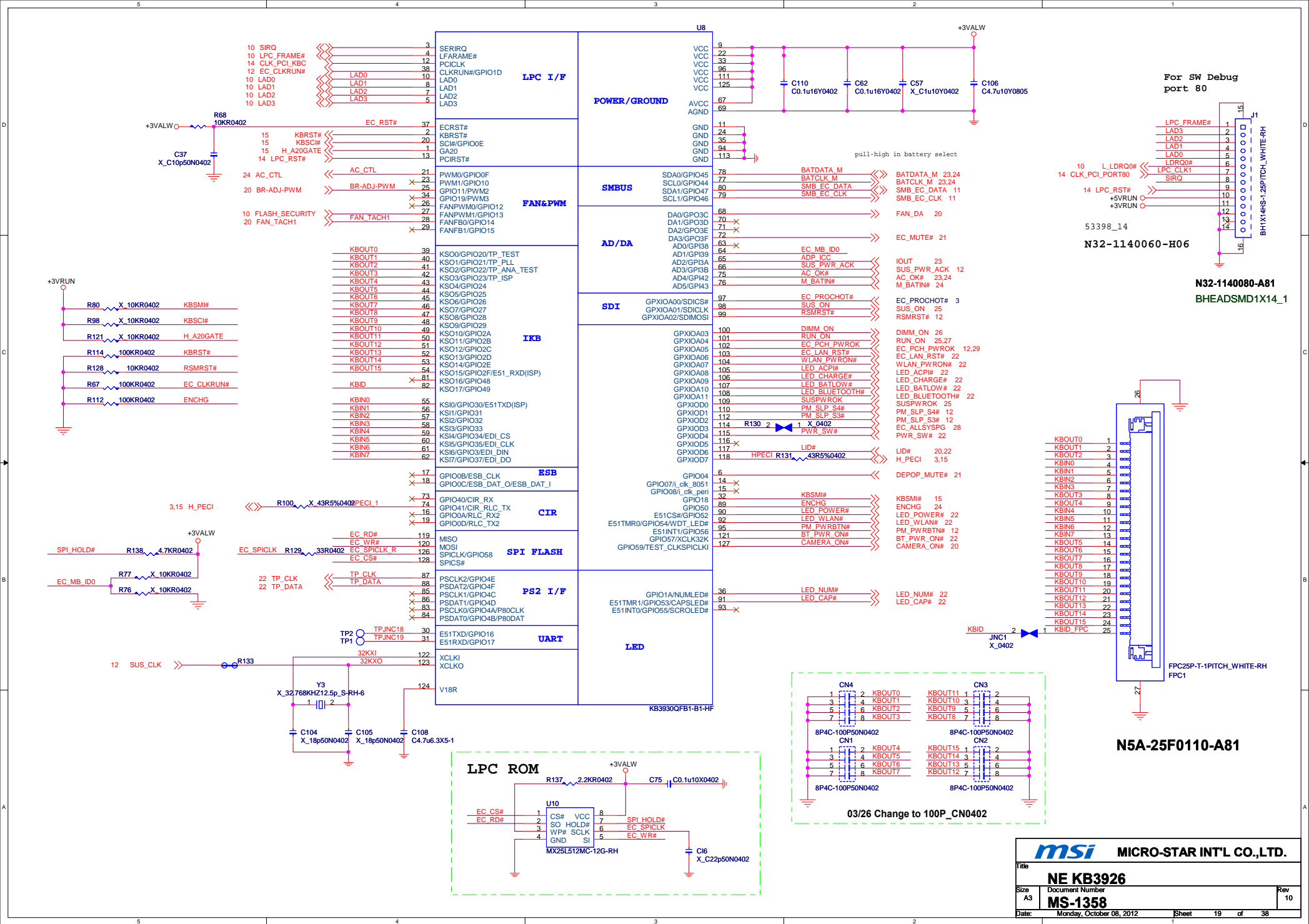


# PANTHER POINT (POWER)

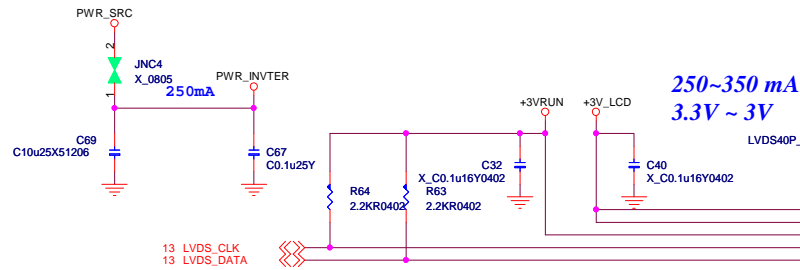
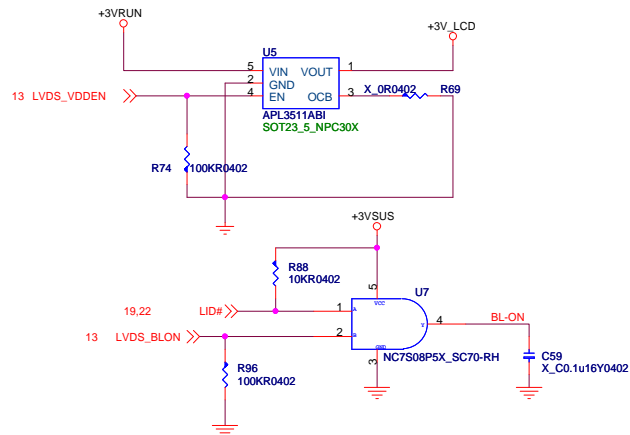


# PANTHER POINT (GND)



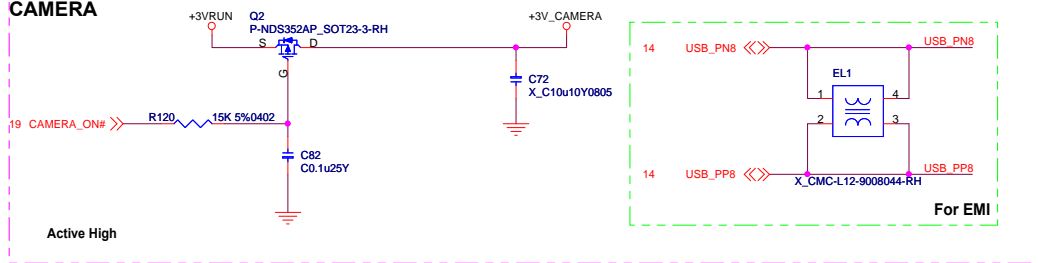


# LVDS POWER

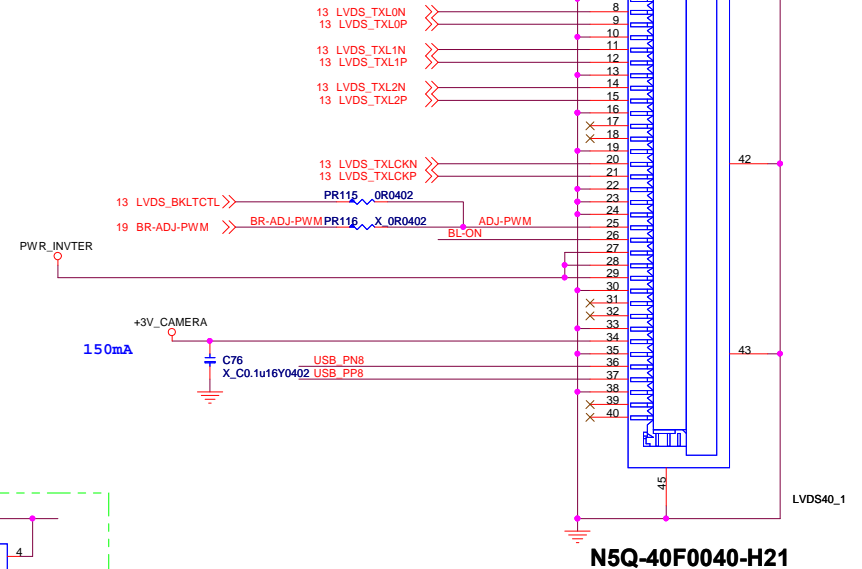


250~350 mA  
3.3V ~ 3V

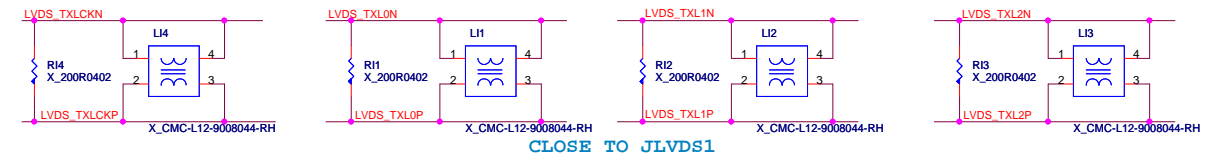
## CAMERA



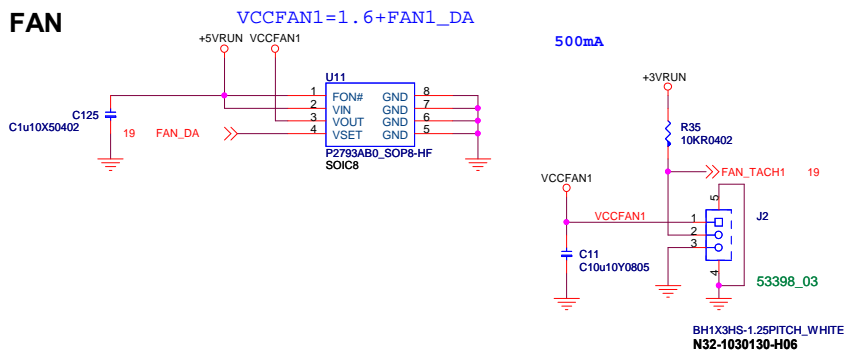
For EMI



N5Q-40F0040-H21



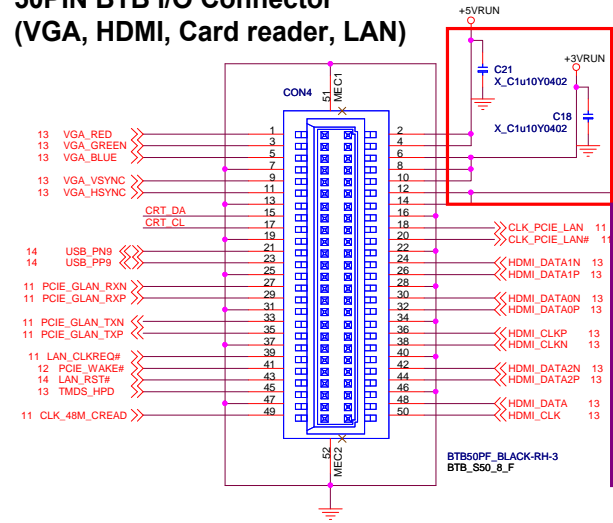
## FAN



msi MICRO-STAR INT'L CO.,LTD.			
Title			
LVDS, Camera, BT, FAN			
Size	Document Number		Rev
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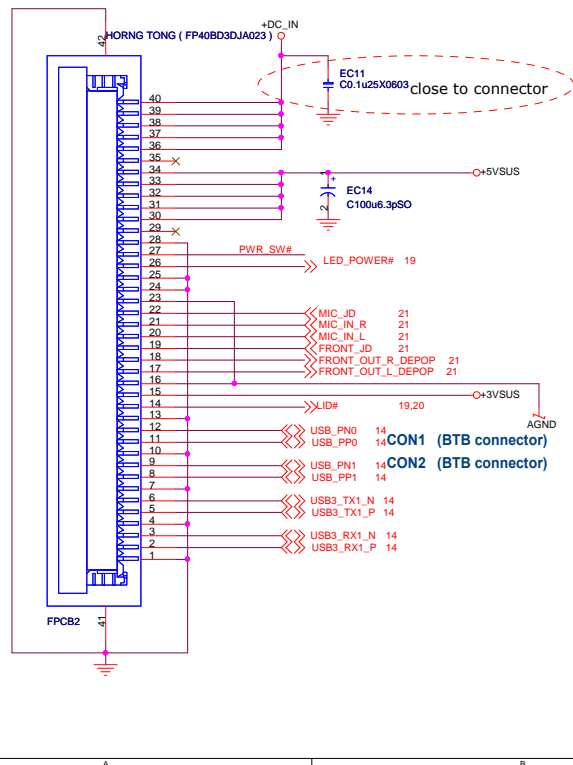


## 50PIN BTB I/O Connector (VGA, HDMI, Card reader, LAN)

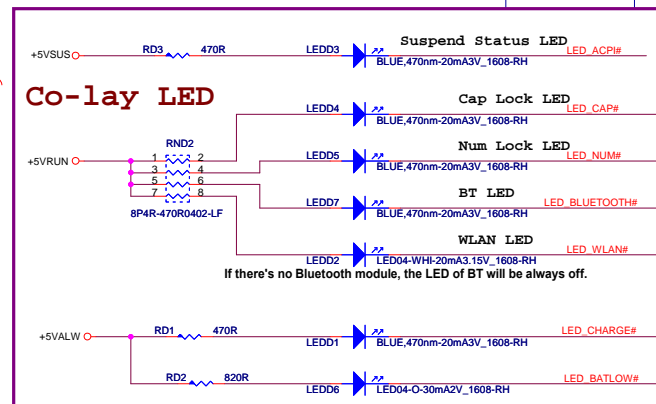


N5C-50F0160-A81

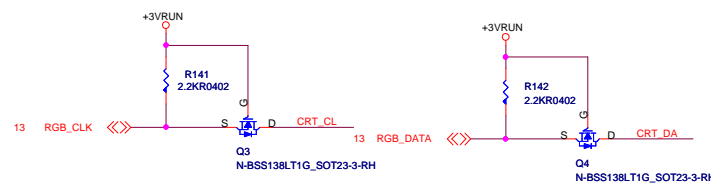
## 40PIN COAXIAL I/O Connector (USB Port x 2, MIC, Earphone)



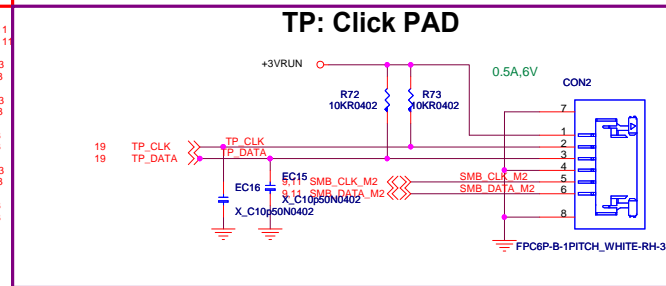
Power on: ON  
S3 state: Blinking  
S4/S5 state: OFF



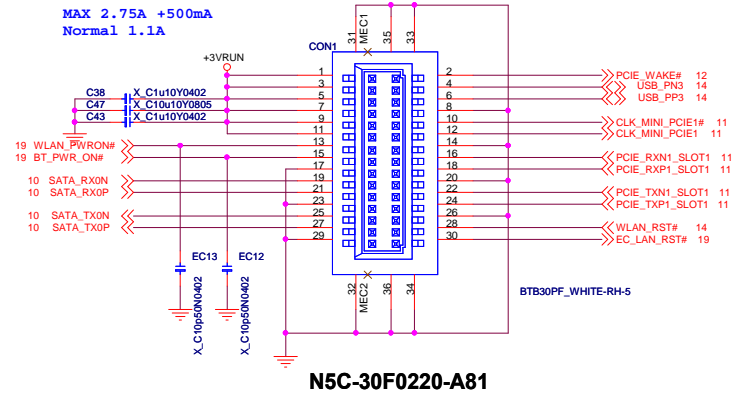
## CRT DDC BUFFER



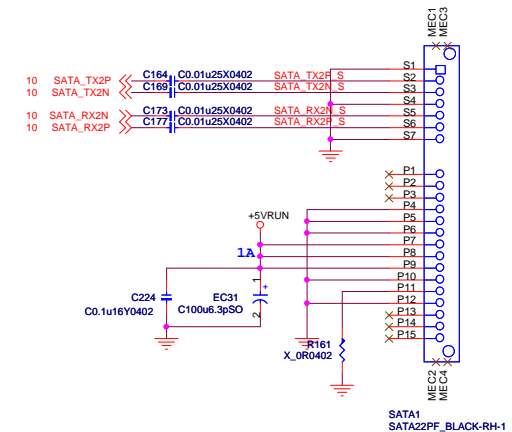
## Launch Board Connector



## MINI PCIE Connector



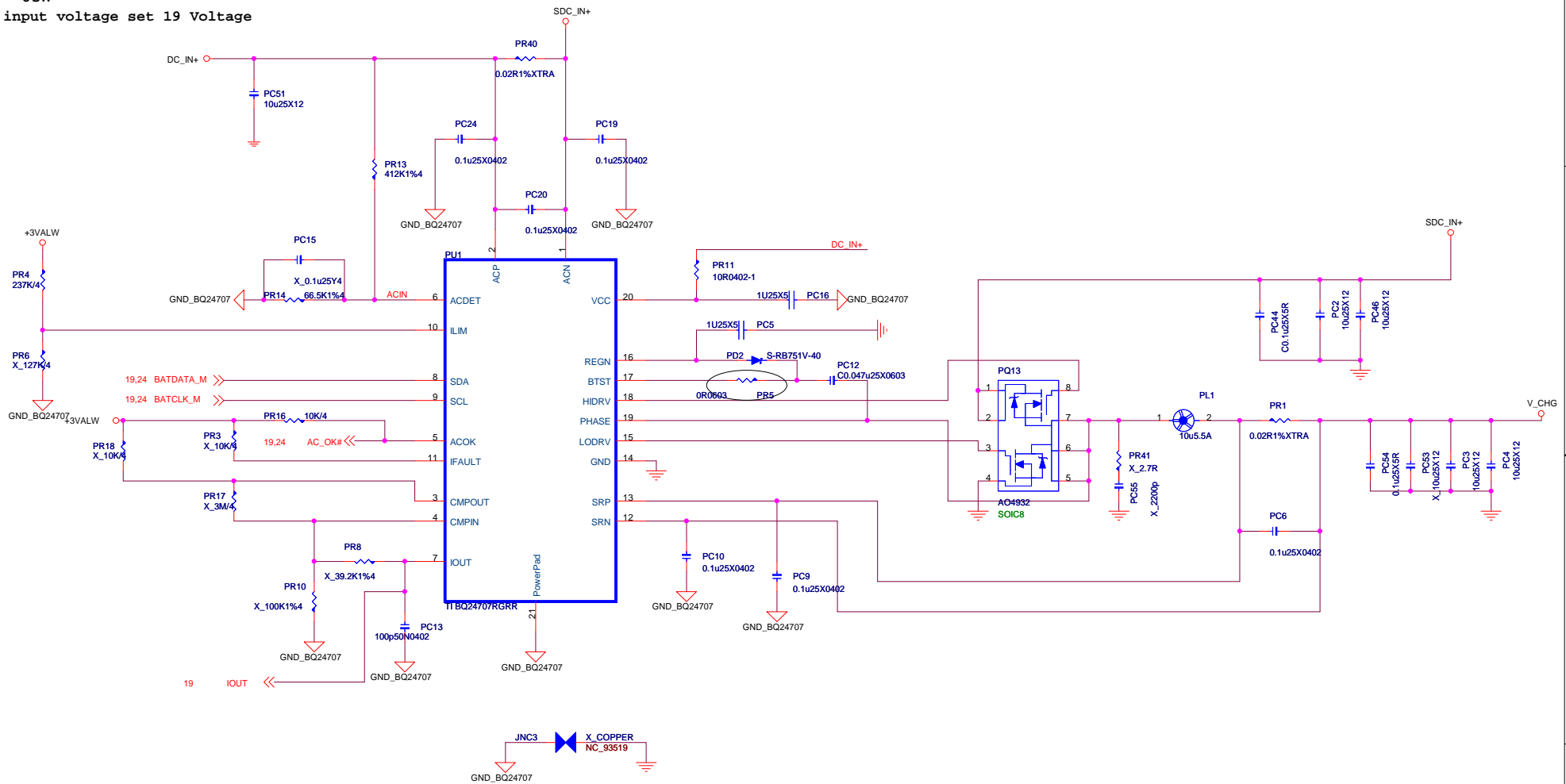
## SATA HDD Connector



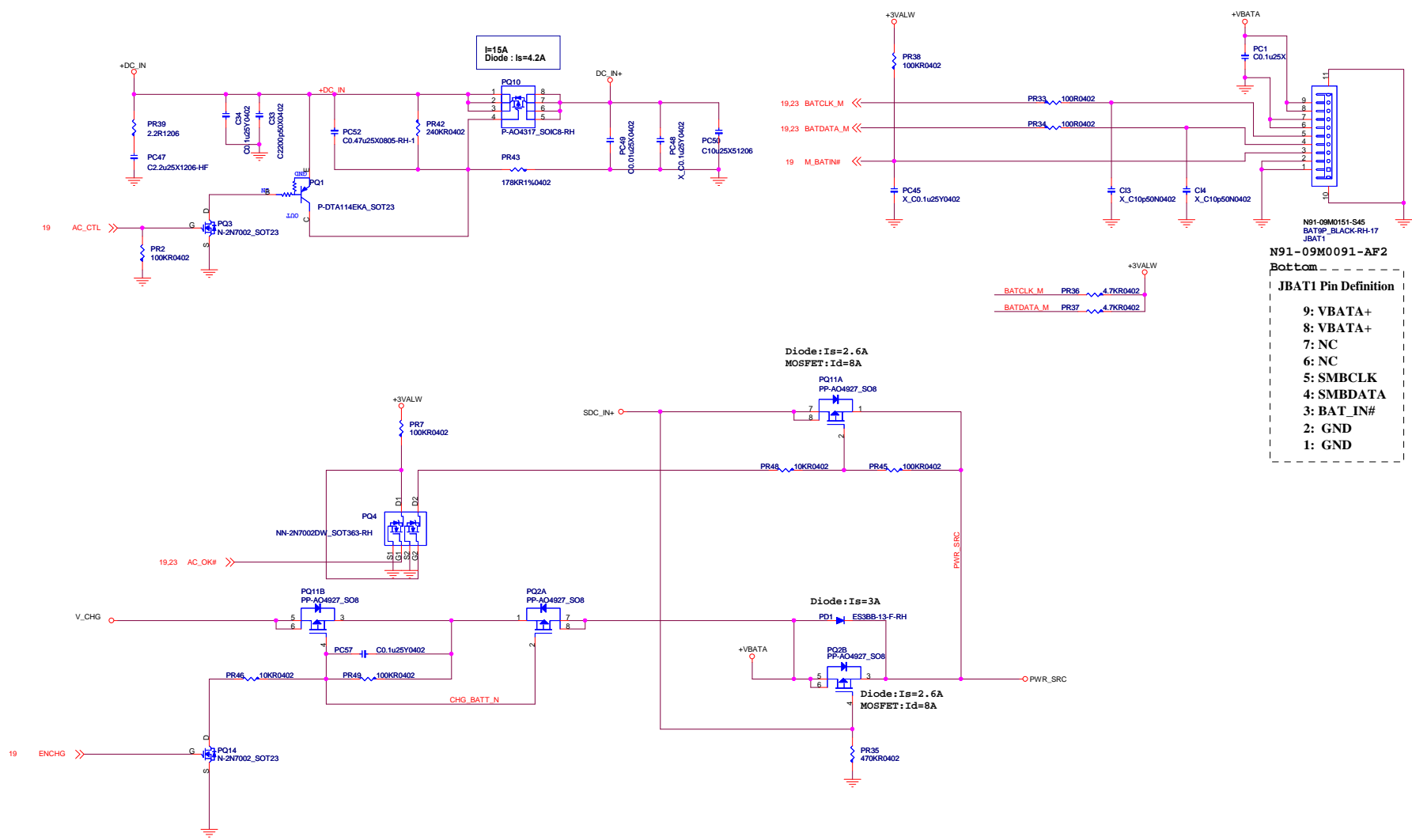
N5N-22F0140-AF2

msi MICRO-STAR INT'L CO.,LTD.	
Title	HDD, BTB CON
Size	Document Number
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Adapter= 65W  
Adapter input voltage set 19 Voltage

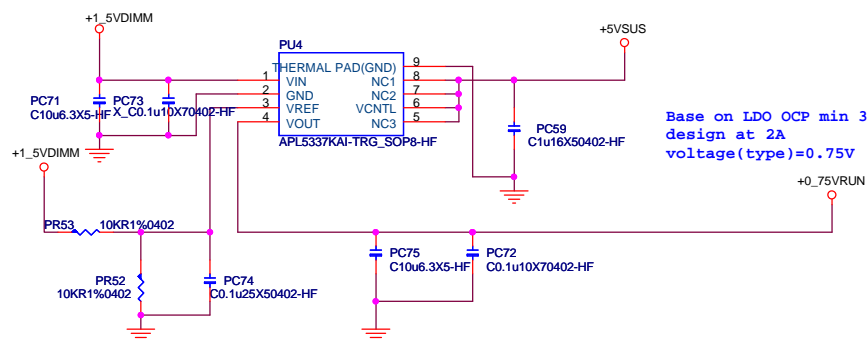
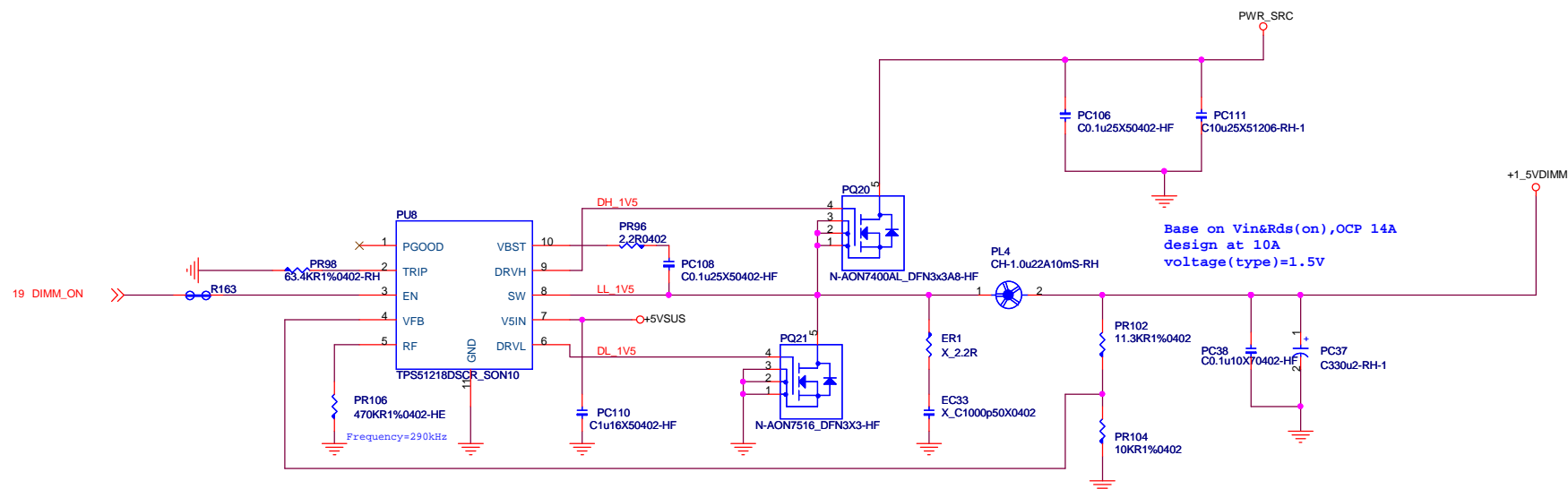



msi MICRO-STAR INT'L CO.,LTD.			
Title			
M Battery Charger			
Size	Document Number	Rev	
A3	MS-1358	10	
Date:	Monday, October 08, 2012	Sheet	23 of 38

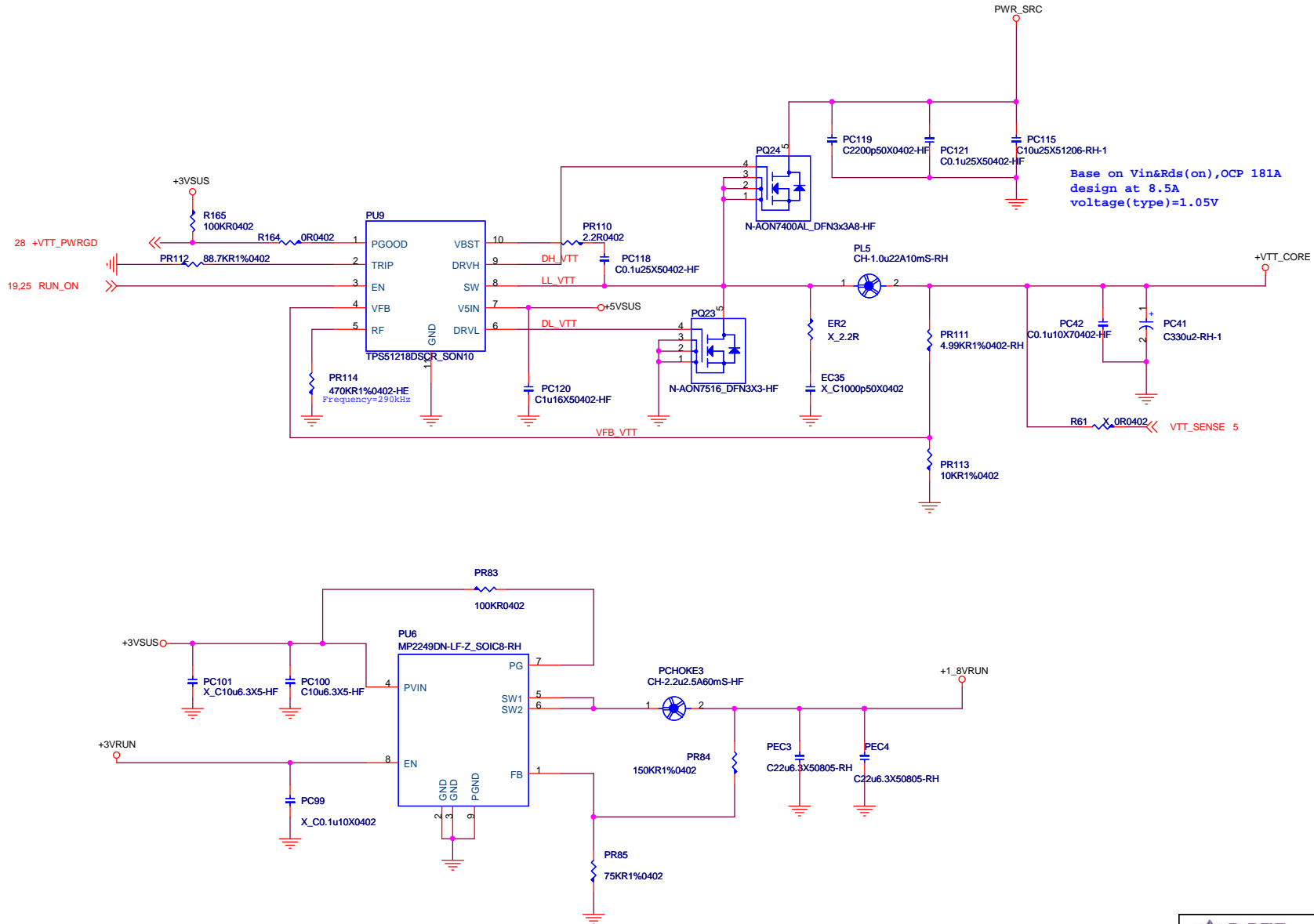










 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>DIMM &amp; SMDR VTERM</b>	
Size	Document Number
B	<b>MS-1358</b>
Date:	Monday, October 08, 2012
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1	

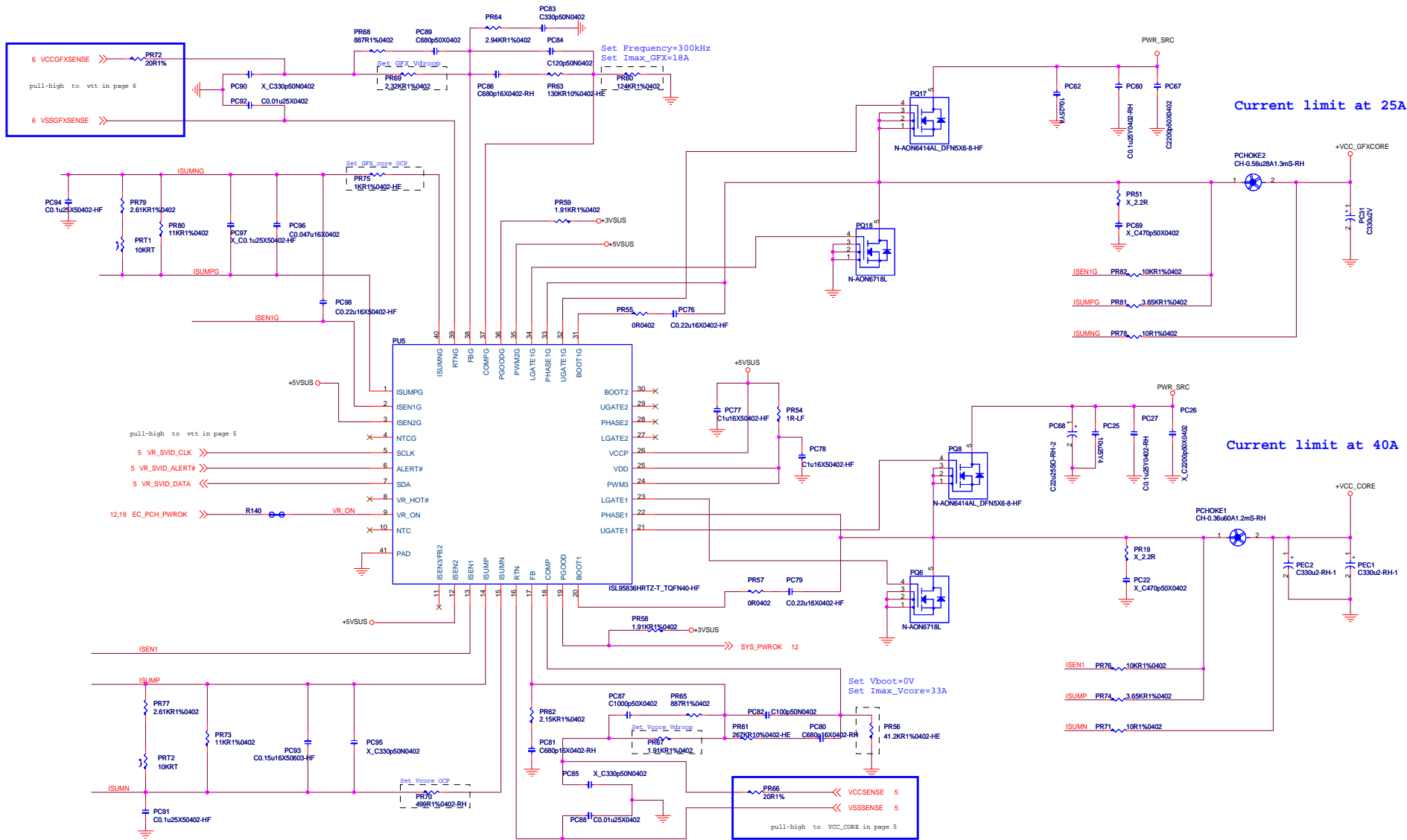


 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>+VTT &amp; +1.05VLAN</b>	
Size	Document Number
B	<b>MS-1358</b>
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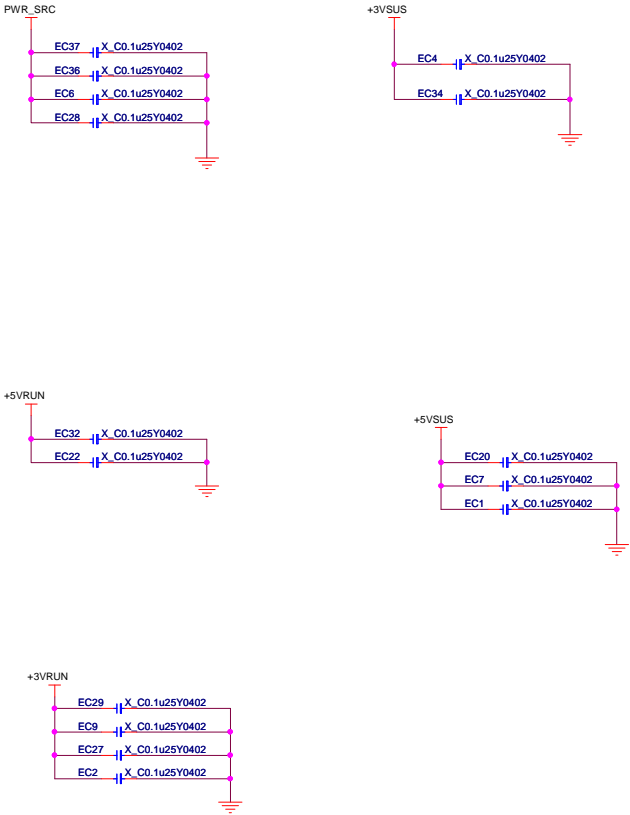
VID STATE		RESULT	
VID1	VID0	VREF	Vout
1	1	VSET1	0.675V
1	0	VSET2	0.725V
0	1	VSET3	0.8V
0	0	VSET4	0.9V

Current limit at 8A for +0.85VRUN  
Imax at 6A

 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>+0.85V</b>	
<b>Size</b> Custom	<b>Document Number</b> <b>MS-1358</b>
<b>Date:</b> Monday, October 08, 2012	<b>Rev</b> 10
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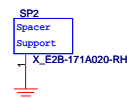
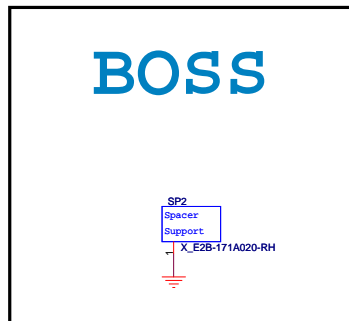
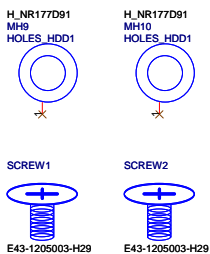
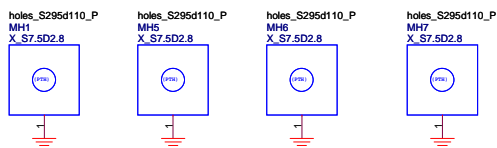
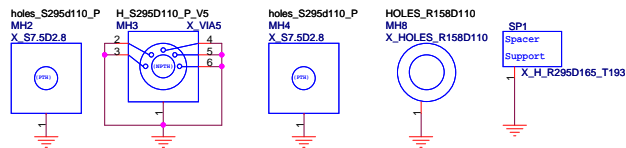
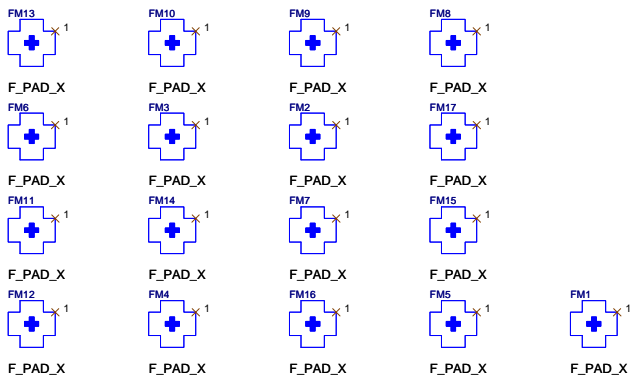
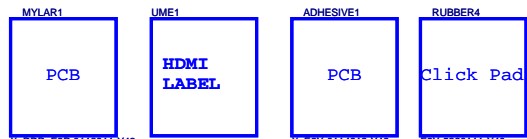
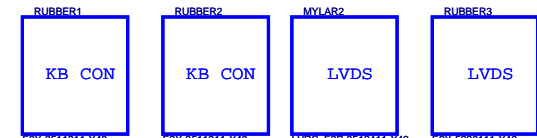


# EMI SOLUTION

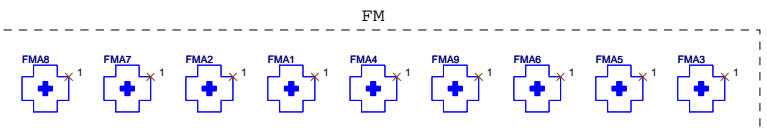
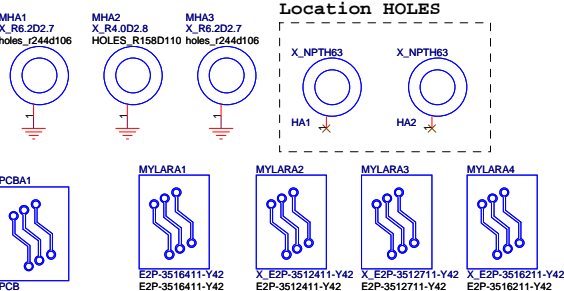
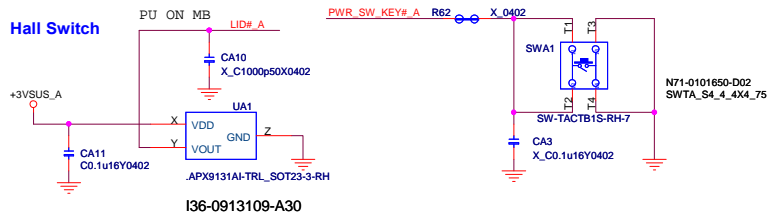




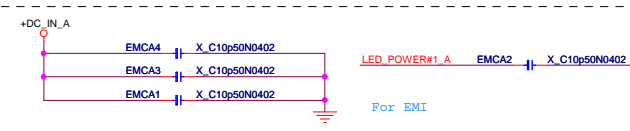
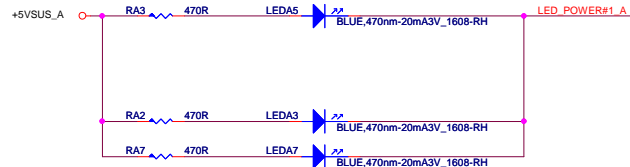
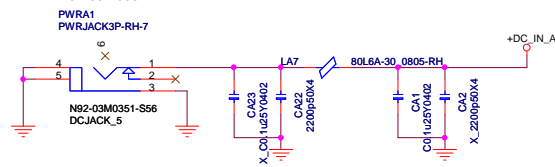
P30-1358110-H73  
P30-1358110-T53,



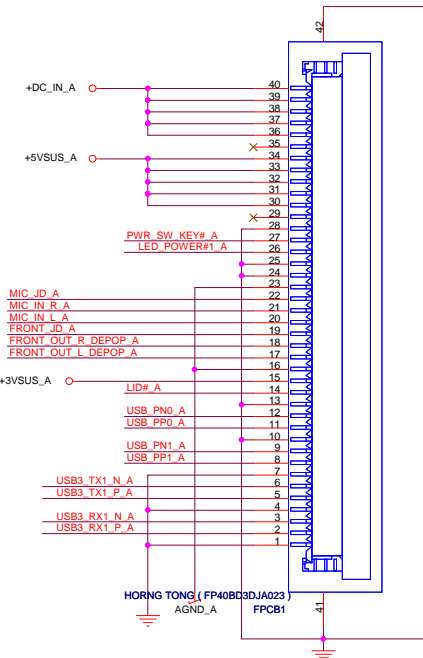
## Hall Switch



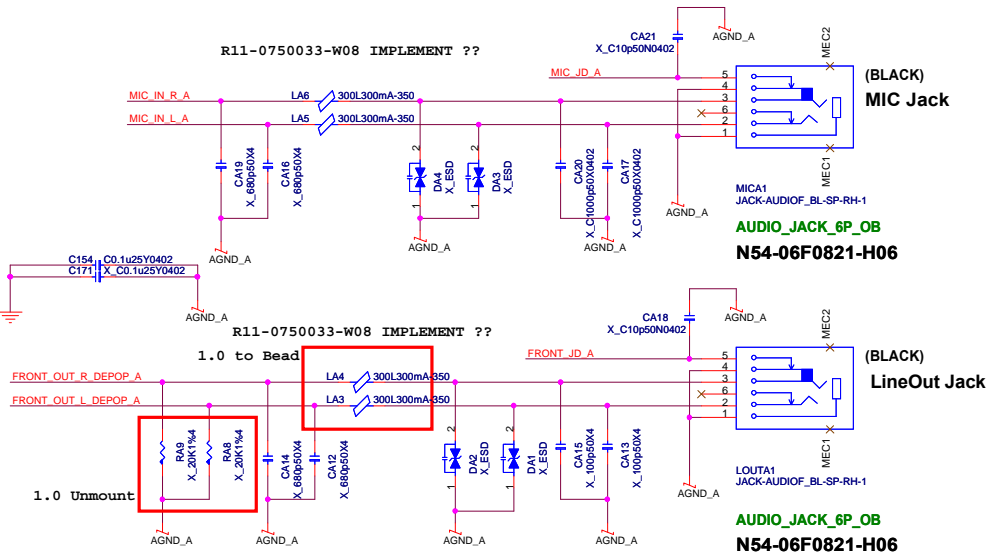
## N92-03M0351-AF2



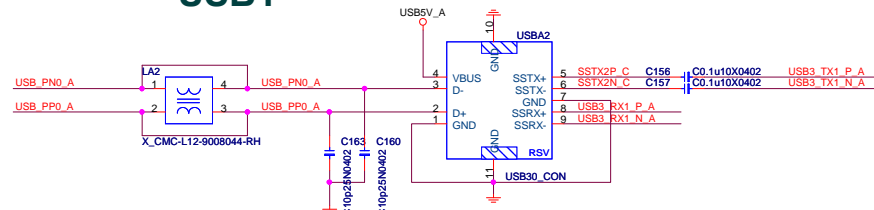
## 40PIN COAXIAL I/O Connector



## R11-0750033-W08 IMPLEMENT ??

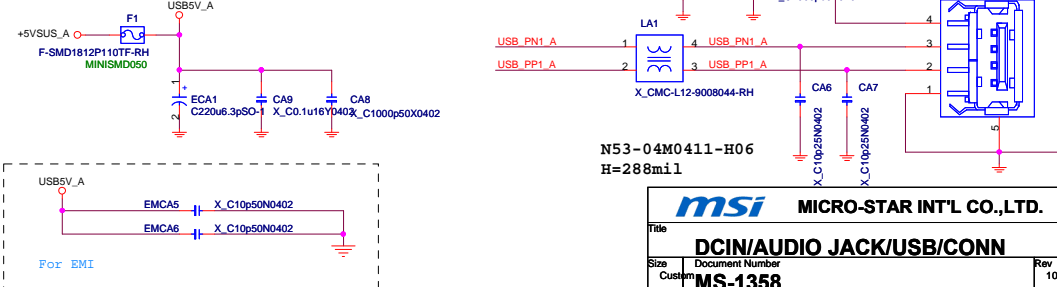


## USB1



teknisi-indonesia

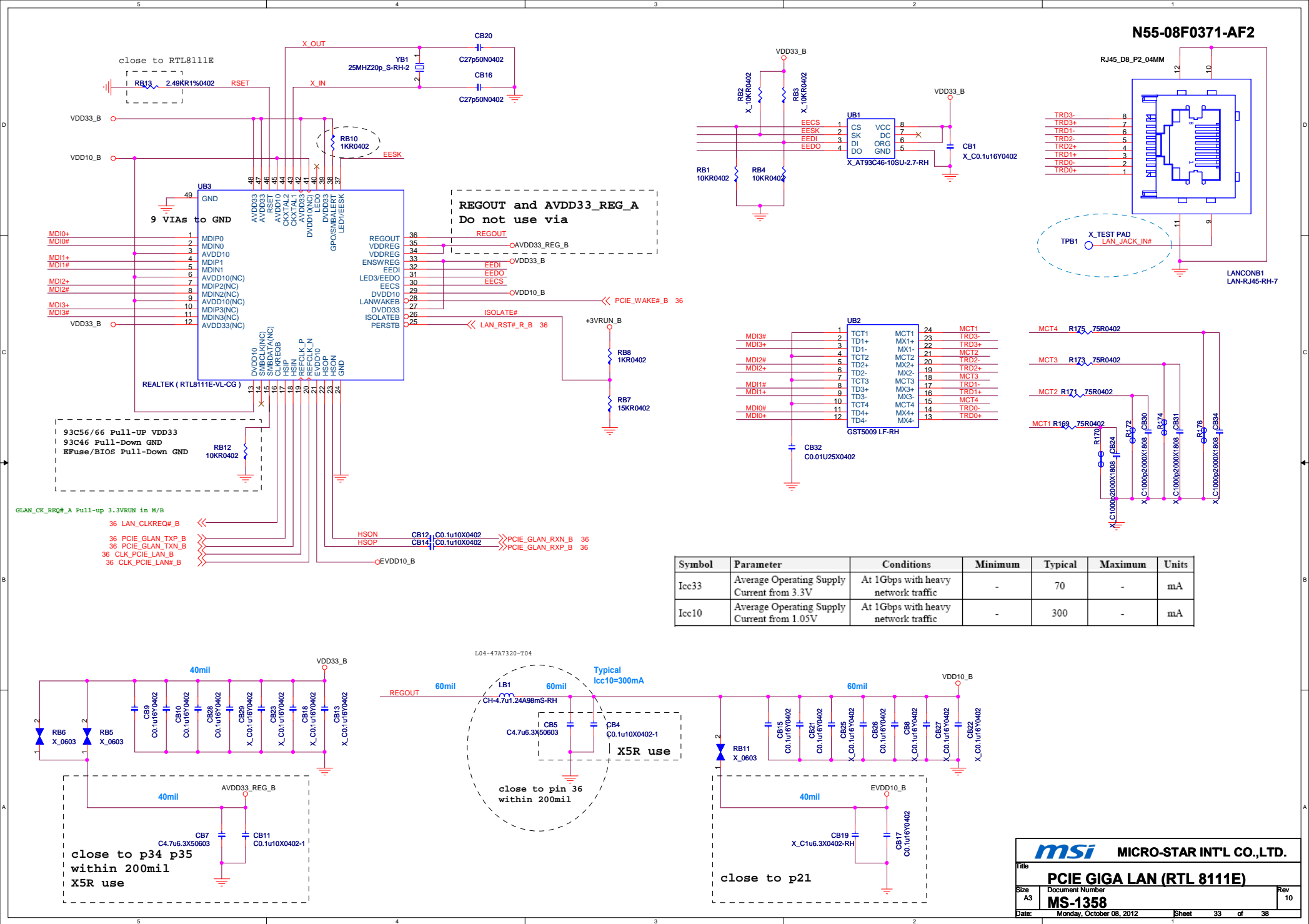
## USB2

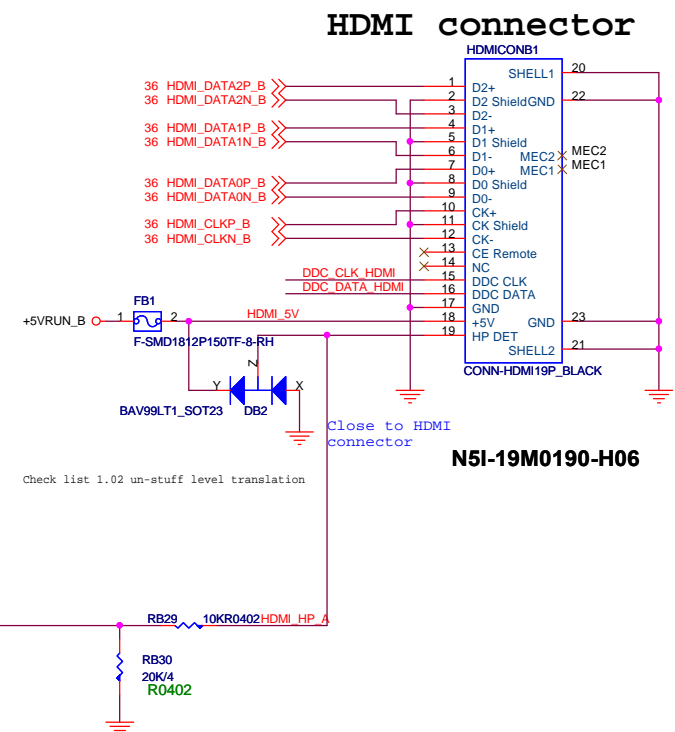


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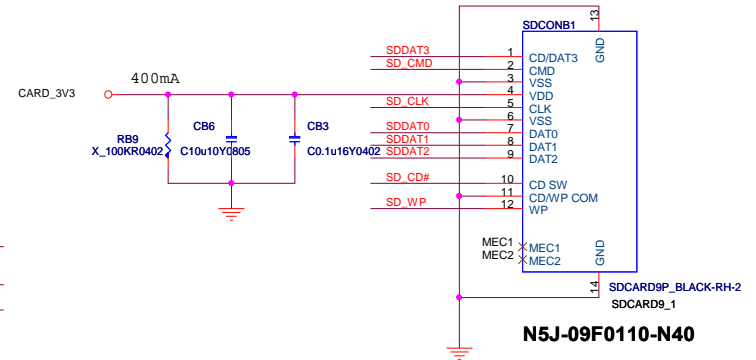
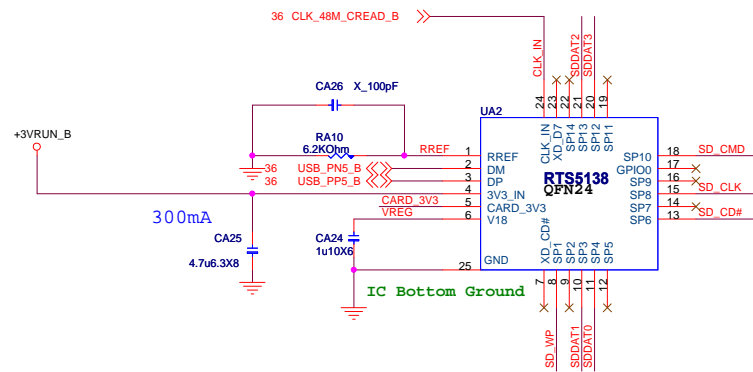
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Card Reader controller  
RTS 5138



Clock	MODE1	MODE0
48MHz	X	X
24MHz	X	○
12MHz (Crystal)	○	○

**50PIN BTB I/O Connector 50PIN**

**N5C-50M0360-A81**

**N59-15F0621-AF2**

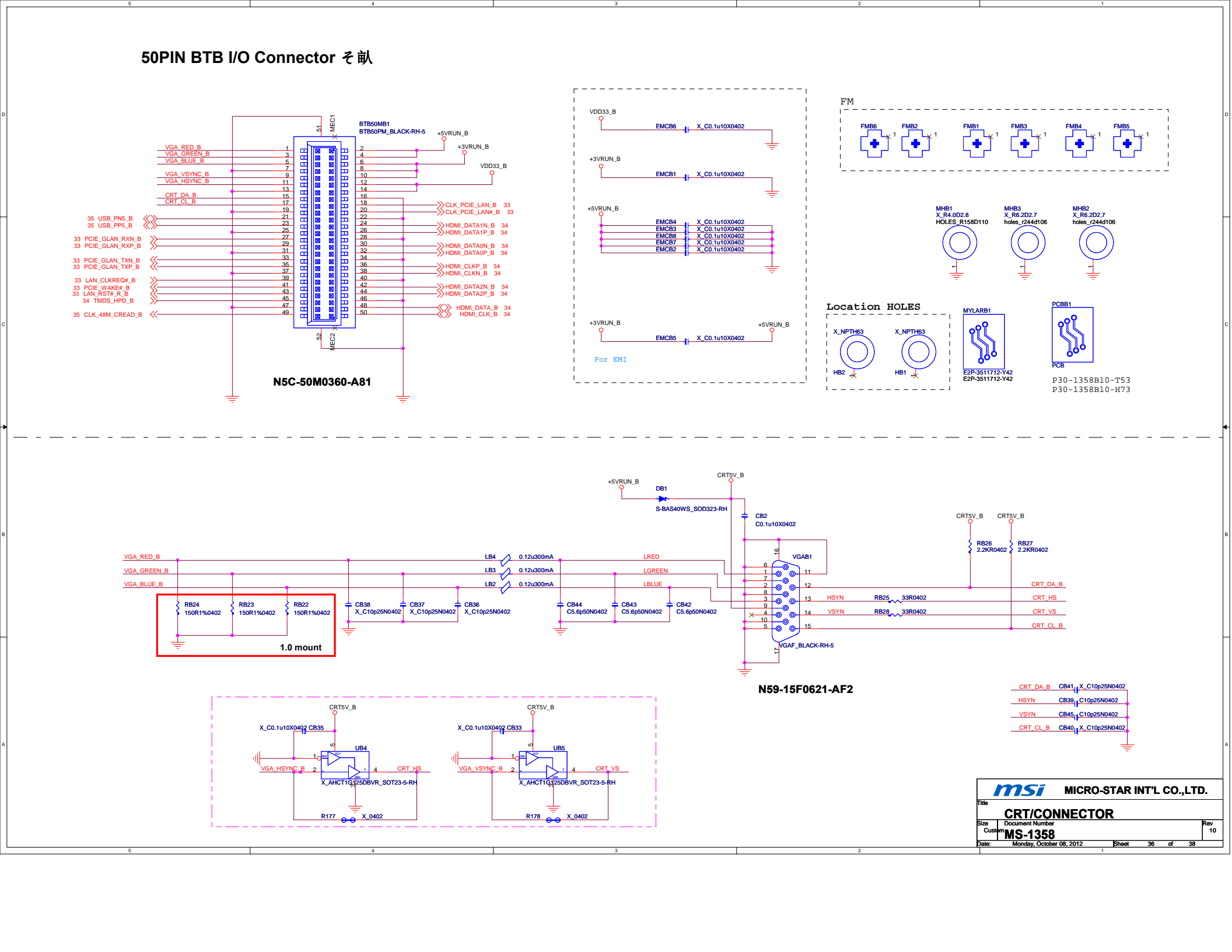
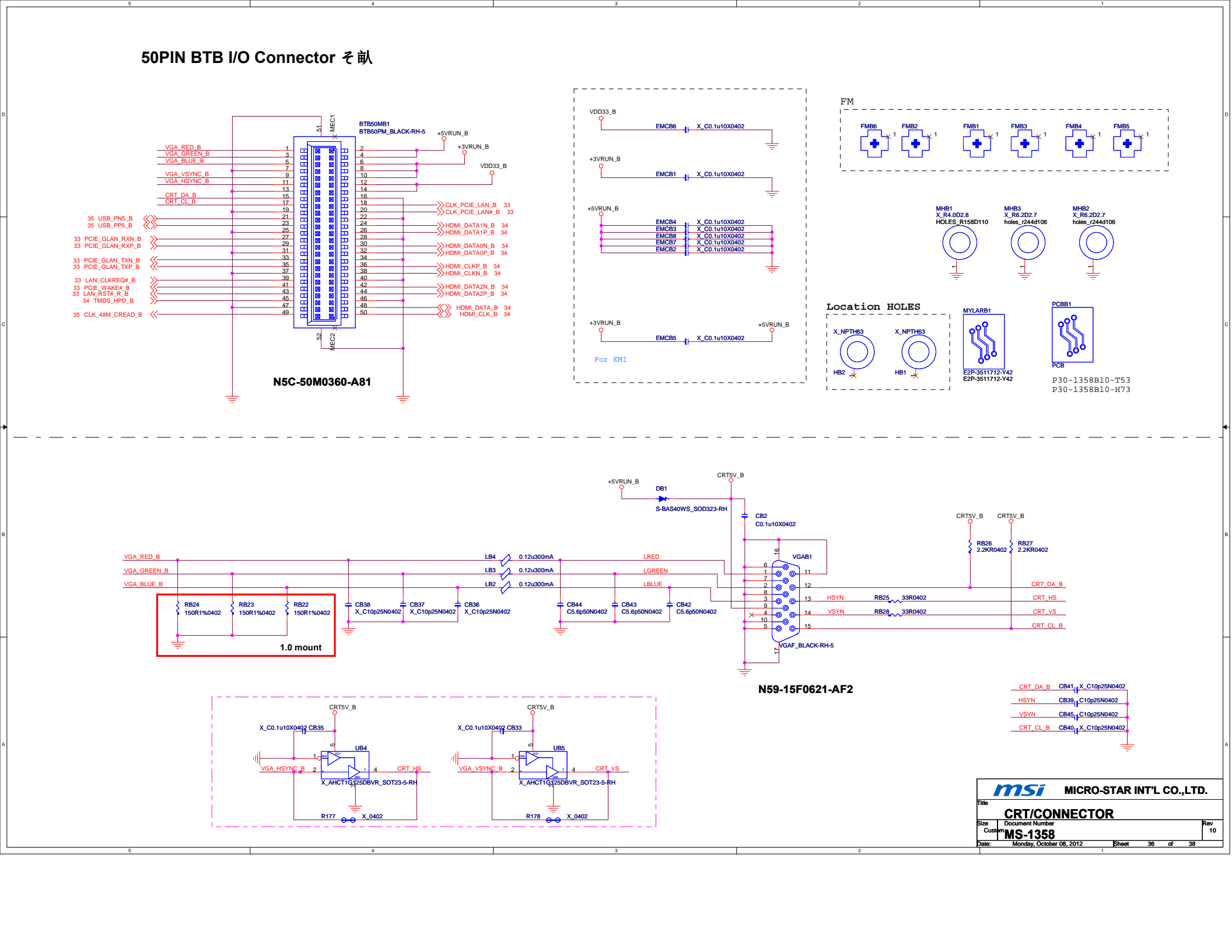
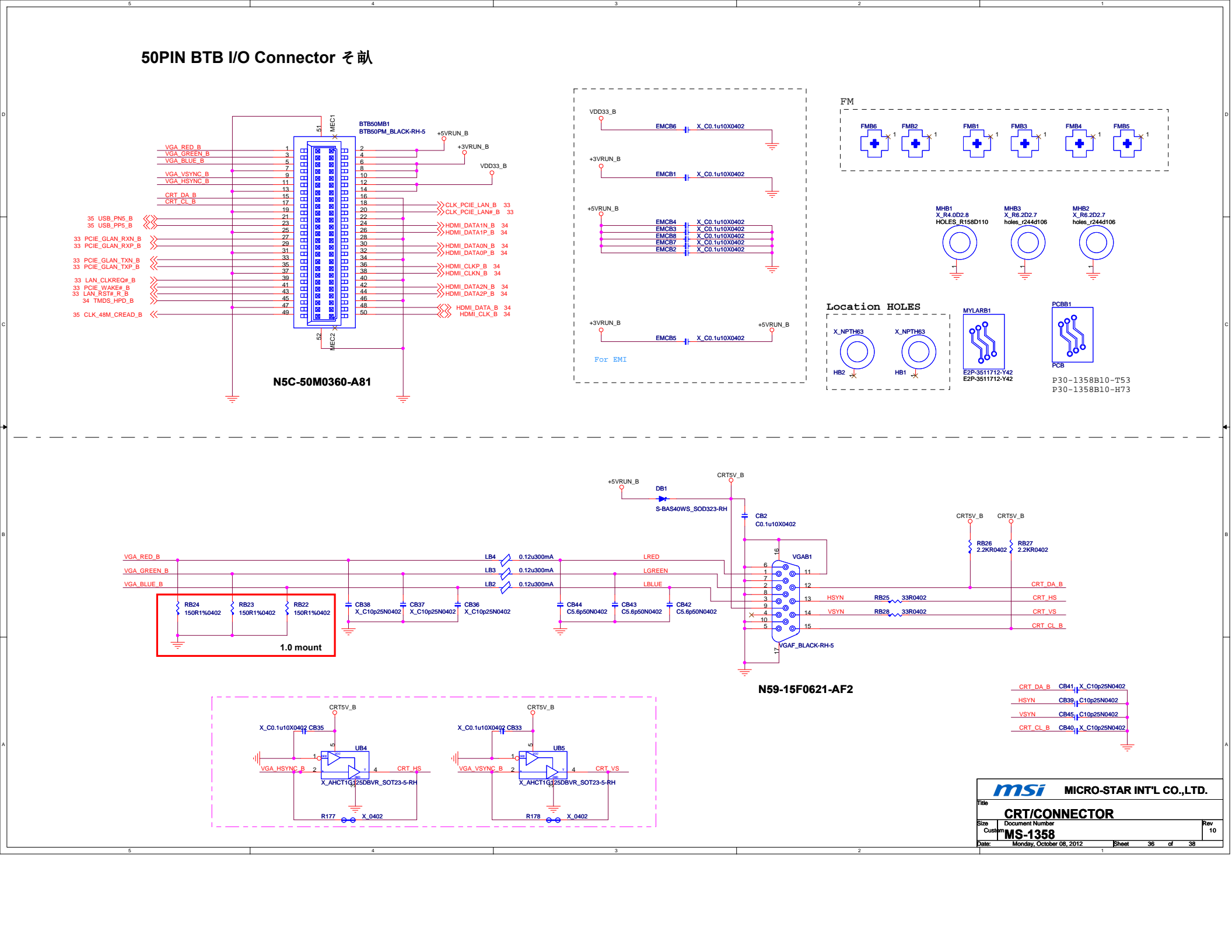
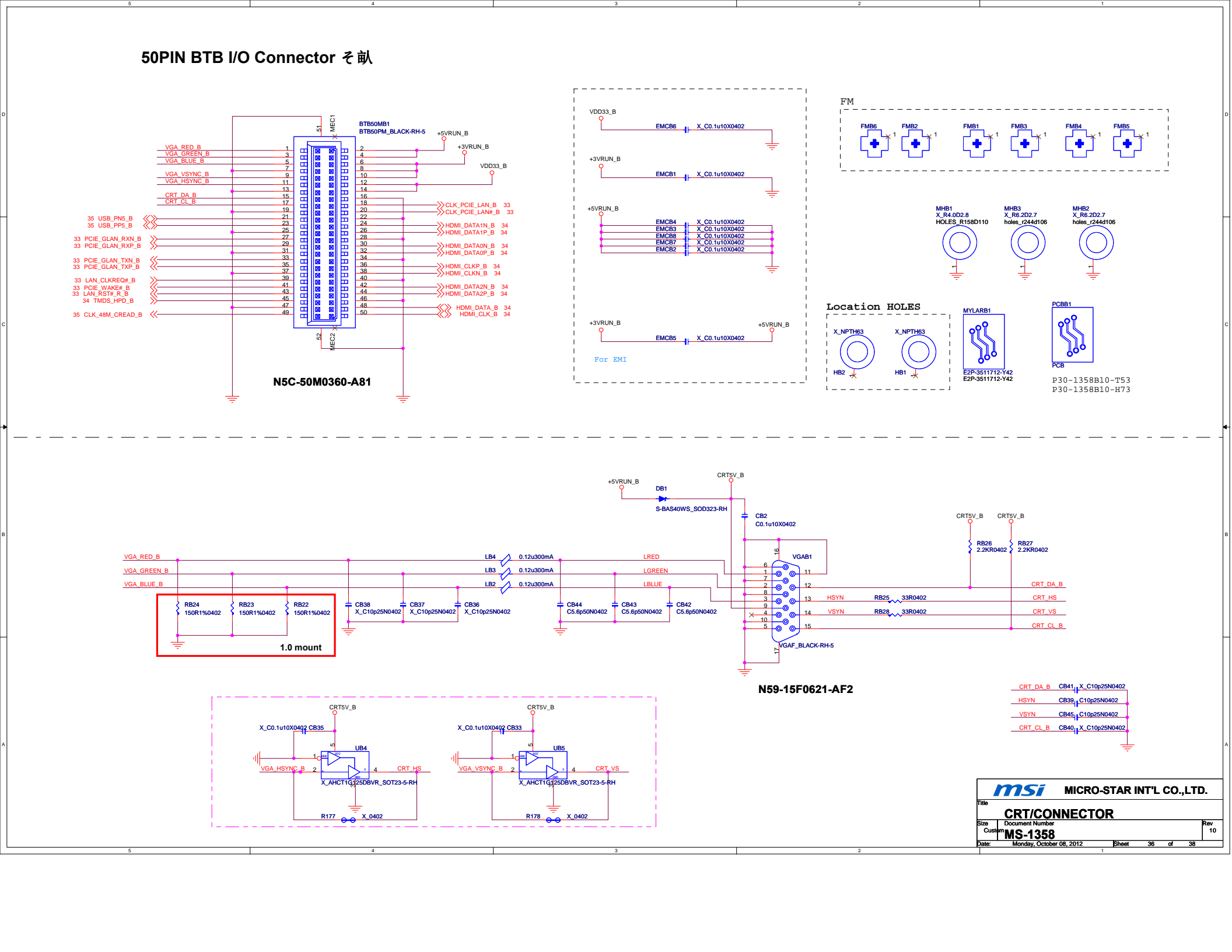
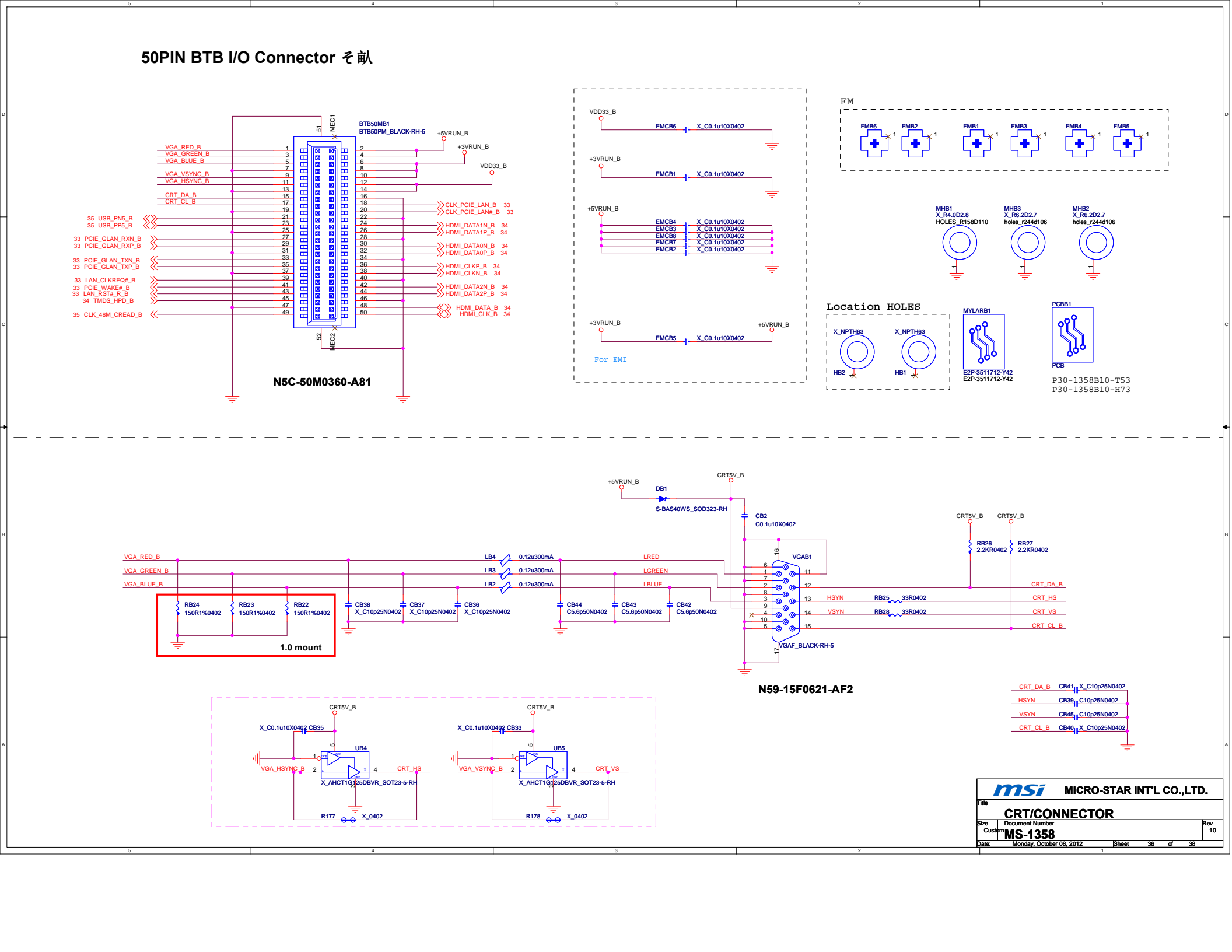
Component	Value
CB2	C0.1u10X0402
CB35	X_C0.1u10X0402
CB36	X_C10p25N0402
CB37	X_C10p25N0402
CB38	X_C10p25N0402
CB42	C5.6p50N0402
CB43	C5.6p50N0402
CB44	C5.6p50N0402
RB22	150R1%0402
RB23	150R1%0402
RB24	150R1%0402
RB25	33R0402
RB26	2.2KR0402
RB27	2.2KR0402
RB28	33R0402

Signal	Component	Value
CRT DA_B	CB41	X_C10p25N0402
HSYN	CB39	C10p25N0402
VSYN	CB45	C10p25N0402
CRT CL_B	CB40	X_C10p25N0402

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**CRT/CONNECTOR**

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**50PIN BTB I/O Connector 接続**

**N5C-50M0360-A81**

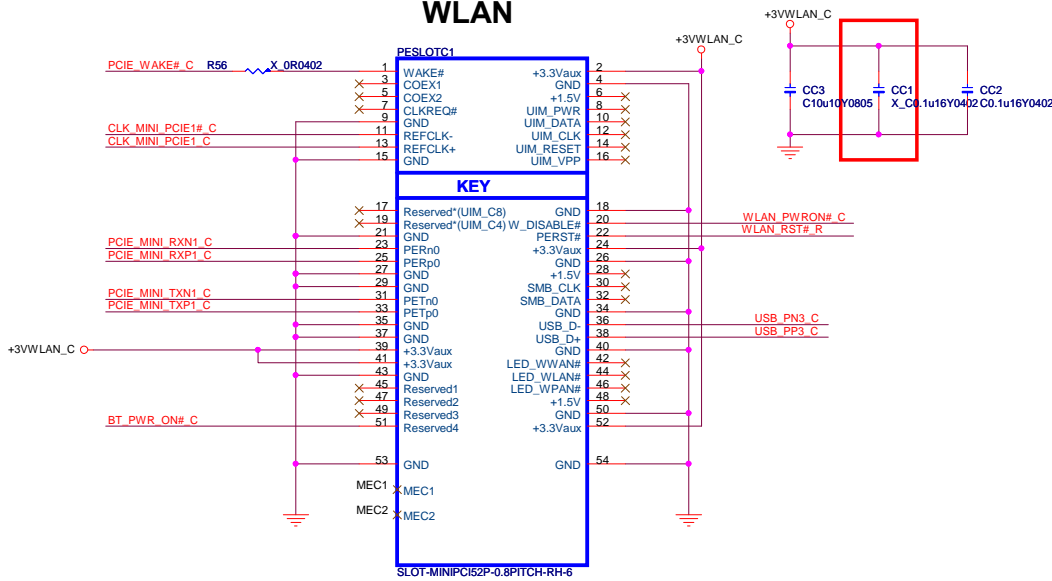
**N59-15F0621-AF2**

**msi MICRO-STAR INT'L CO.,LTD.**

**CRT/CONNECTOR**

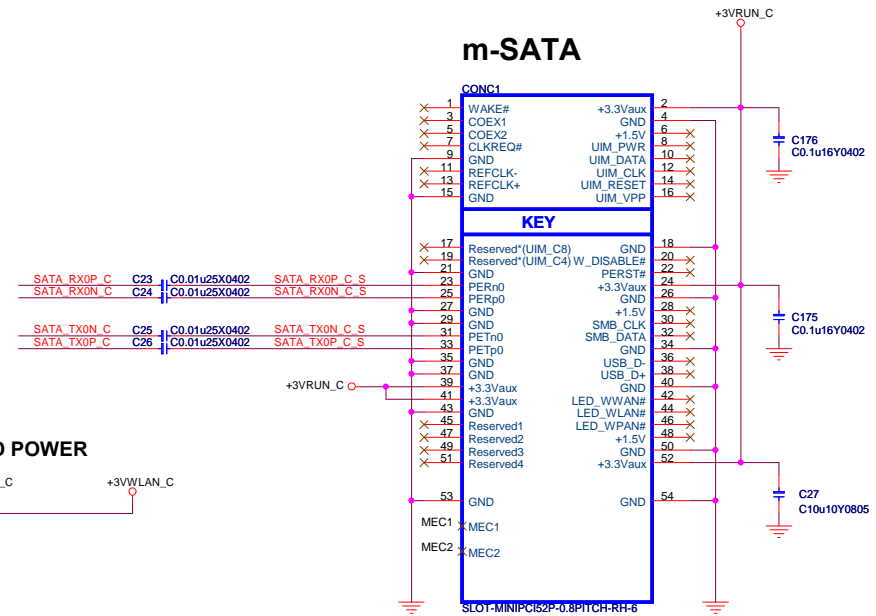
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## WLAN



N11-0520450-L41

## m-SATA



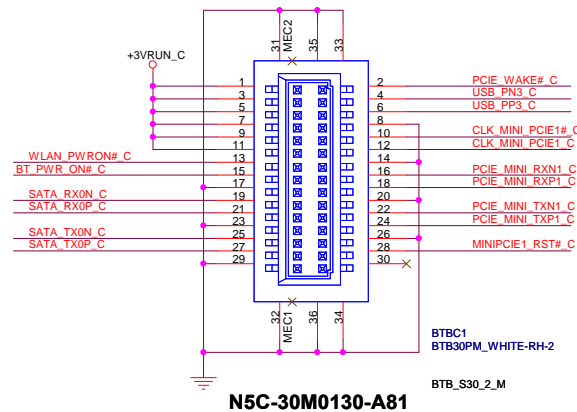
N11-0520210-K06

## AW-NE785H Pin-out Definitions

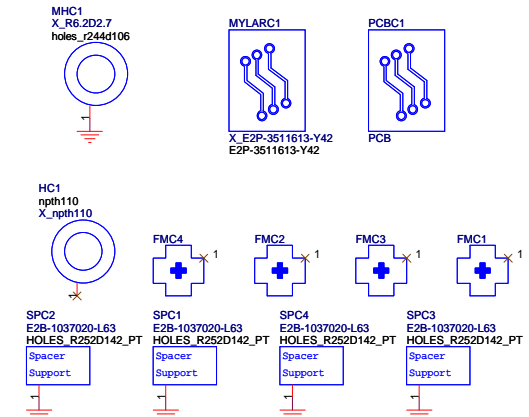
Pin No.	Definition	Basic Description	Type
1	NC	No connect. Should be left open.	
2	3.3v	3.3V power supply.	VCC
3	NC	No connect. Should be left open.	
4	GND	Ground	GND
5	NC	No connect. Should be left open.	
6	NC	No connect. Should be left open.	
7	CLKREQ_L	Reference clock request.	
8	NC	No connect. Should be left open.	
9	GND	Ground	GND
10	NC	No connect. Should be left open.	
11	REFCLK-	Differential reference clock	
12	NC	No connect. Should be left open.	
13	REFCLK+	Differential reference clock	
14	NC	No connect. Should be left open.	
15	GND	Ground	GND
16	NC	No connect. Should be left open.	
17	NC	No connect. Should be left open.	
18	GND	Ground	GND
19	NC	No connect. Should be left open.	
20	W_DISABLE_L	WLAN disable control.	Input
21	GND	Ground	GND
22	PERST_L	PCI express fundamental reset	Input
23	PERn0	Differential transmit	Output
24	NC	No connect. Should be left open.	
25	PERp0	Differential transmit	Output
26	GND	Ground	GND
27	GND	Ground	GND
28	NC	No connect. Should be left open.	
29	GND	Ground	GND
30	NC	No connect. Should be left open.	
31	PETn0	Differential receive	Input
32	NC	No connect. Should be left open.	
33	PETp0	Differential receive	Input
34	GND	Ground	GND
35	GND	Ground	GND
36	NC	No connect. Should be left open.	
37	GND	Ground	GND
38	NC	No connect. Should be left open.	
39	NC	No connect. Should be left open.	
40	GND	Ground	GND
41	NC	No connect. Should be left open.	
42	NC	No connect. Should be left open.	
43	NC	No connect. Should be left open.	
44	LED_WLAN_L	Active low signal. The signal is used to provide status indicators via LED.	Output
45	NC	No connect. Should be left open.	
46	NC	No connect. Should be left open.	
47	NC	No connect. Should be left open.	
48	NC	No connect. Should be left open.	
49	NC	No connect. Should be left open.	
50	GND	Ground	GND
51	NC	No connect. Should be left open.	
52	3.3v	3.3V power supply	VCC

WLAN\_RST#\_R

MINIPCIE1\_RST#\_C



N5C-30M0130-A81



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MINIPCIE Board		
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